Using the TPS59640EVM-751 IMVP-7, 3-Phase CPU/1-Phase GPU SVID Power System

The TPS59640EVM-751 evaluation module (EVM) is a complete solution for the Intel™ IMVP-7 Serial VID (SVID) Power System from a 9-V to 20-V input bus. This EVM uses the TPS59640 for IMVP-7 3-Phase CPU and 1-Phase GPU Vcore, TPS51219 for 1.05VCCIO, TPS51916 for DDR3L/DDR4 memory rail (1.2VDDQ, 0.6VTT, and 0.6VTTREF). The TPS59640EVM-751 also uses the 5-mm x 6-mm TI power block MOSFET (CSD87350Q5D) for high-power density and superior thermal performance.

Contents

1 Description 4
1.1 Typical Applications 4
1.2 Features 4
2 TPS59640EVM-751 Power System Block Diagram 5
3 Electrical Performance Specifications 6
4 Schematic 8
5 Test Setup 21
5.1 Test Equipment 21
5.2 Recommended Wire Gage 22
5.3 Recommended Test Setup 22
5.4 USB Cable Connections 23
5.5 Input Connections 23
5.6 Output Connections 24
6 Configuration 24
6.1 CPU and GPU Configuration 24
6.2 1.2VDDQ, 0.6V VTT and 0.6V VTTREF Configuration 27
6.3 1.05V VCCIO Configuration 27
7 Test Procedure 28
7.1 Line/Load Regulation and Efficiency Measurement Procedure 28
7.2 Equipment Shutdown 31
8 Performance Data and Typical Characteristic Curves 32
8.1 CPU3-Phase Operation 32
8.2 CPU 2-Phase Operation 36
8.3 CPU 1-Phase Operation 40
8.4 GPU Operation 44
8.5 1.05V VCCIO 48
8.6 1.2 VDDQ 51
9 EVM Assembly Drawings and PCB layout 53
10 Bill of Materials 59

List of Figures

1 TPS59640EVM-751 Power System Block Diagram 5
2 TPS59640EVM-751 EVM Illustration 6
3 TPS59640EVM-751 Schematic (1 of 13) 8
4 TPS59640EVM-751 Schematic (2 of 13) 9

Intel is a trademark of Intel Corporation.
Windows is a trademark of Microsoft Corporation.

Copyright © 2012, Texas Instruments Incorporated

5 TPS59640EVM-751 Schematic (3 of 13) 10
6 TPS59640EVM-751 Schematic (4 of 13) 11
7 TPS59640EVM-751 Schematic (5 of 13) 12
8 TPS59640EVM-751 Schematic (6 of 13) 13
9 TPS59640EVM-751 Schematic (7 of 13) 14
10 TPS59640EVM-751 Schematic (8 of 13) 15
11 TPS59640EVM-751 Schematic (9 of 13) 16
12 TPS59640EVM-751 Schematic (10 of 13) 17
13 TPS59640EVM-751 Schematic (11 of 13) 18
14 TPS59640EVM-751 Schematic (12 of 13) 19
15 TPS59640EVM-751 Schematic (13 of 13) 20
16 USB Cable 21
17 TPS59640EVM-751 Recommended Test Setup 23
18 TPS59640EVM-751 CPU GUI Setup Window 29
19 TPS59640EVM-751 GPU GUI Setup Window 30
20 CPU3 Efficiency 32
21 CPU3 Load Regulation 32
22 CPU3 Enable Turnon 32
23 CPU3 Enable Turnoff 32
24 CPU3 Switching Node (Ripple) 32
25 CPU3 Dynamic VID: SetVID-Slow/Slow 32
26 CPU3 Dynamic VID:SetVID-Fast/Fast 33
27 CPU3 Dynamic VID:SetVID-Decay/Fast 33
28 CPU3 Output Load Insertion With OSR/USR20k (Min) 33
29 CPU3 Output Load Release With OSR/USR 20k (Min) 33
30 CPU3 Bode Plot at 12Vin, 1.05 V/60 A 34
31 CPU3 MOSFET 34
32 CPU3 IC 34
33 CPU2 Efficiency 36
34 CPU2 Load Regulation 36
35 CPU2 Enable Turnon 36
36 CPU2 Enable Turnoff 36
37 CPU2 Switching Node (Ripple) 36
38 CPU2 Dynamic VID: SetVID-Slow/Slow 36
39 CPU2 Dynamic VID: SetVID-Fast/Fast 37
40 CPU2 Dynamic VID: SetVID-Decay/Fast 37
41 CPU2 Output Load Insertion With OSR/USR 20k (Min) 37
42 CPU2 Output Load Release With OSR/USR 20k (Min) 37
43 CPU2 Bode Plot at 12Vin, 1.05 V/55 A 38
44 CPU2 MOSFET 38
45 CPU2 IC 38
46 CPU1 Efficiency 40
47 CPU1 Load Regulation 40
48 CPU1 Enable Turnon 40
49 CPU1 Enable Turnoff 40
50 CPU1 Switching Node 40
51 CPU1 Switching Node and Ripple 40
52 CPU1 Dynamic VID: SetVID-Slow/Slow 41
53 CPU1 Dynamic VID: SetVID-Fast/Fast 41

Copyright © 2012, Texas Instruments Incorporated

54 CPU1 Dynamic VID: SetVID-Decay/Fast 41
55 CPU1 Output Load Insertion With OSR/USR 20k (Min) 41
56 CPU1 Output Load Release With OSR/USR 20k (Min) 42
57 CPU1 Bode Plot at 12Vin, 1.05 V/33 A 43
58 CPU1 MOSFET 43
59 CPU1 IC 43
60 GPU Efficiency 44
61 GPU Load Regulation 44
62 GPU Enable Turnon 44
63 GPU Enable Turnoff 44
64 GPU Switching Node 44
65 GPU Switching Node and Ripple 44
66 GPU Dynamic VID: SetVID-Slow/Slow 45
67 GPU Dynamic VID: SetVID-Fast/Fast 45
68 GPU Dynamic VID: SetVID-Decay/Fast 45
69 GPU Output Load Insertion With OSR/USR 20k (Min) 45
70 GPU Output Load Release With OSR/USR 20k (Min) 46
71 GPU Bode Plot at 12Vin, 1.23 V/33 A 47
72 GPU MOSFET 47
73 GPU IC 47
74 1.05-V Efficiency 48
75 1.05-V Load Regulation 48
76 1.05-V Enable Turnon 48
77 1.05-V Enable Turnoff 48
78 1.05-V Switching Node 48
79 1.05-V Ripple 48
80 1.05-V Transient DCM to CCM 49
81 1.05-V Transient CCM to DCM 49
82 TPS51219 Thermal 49
83 1.2-V Efficiency 51
84 1.2-V Load Regulation 51
85 1.2-V Enable Turnon 51
86 1.2-V Enable Turnoff 51
87 1.2-V Switching Node 51
88 1.2-V Ripple 51
89 1.2-V Transient DCM to CCM 52
90 1.2-V Transient CCM to DCM 52
91 TPS51916 Thermal 52
92 TPS59640EVM-751 Top Layer Assembly Drawing (Top View) 53
93 TPS59640EVM-751 Bottom Assembly Drawing (Bottom View) 54
94 TPS59640EVM-751 Top Copper 54
95 TPS59640EVM-751 Bottom Copper 55
96 TPS59640EVM-751 Internal Layer 2 55
97 TPS59640EVM-751 Internal Layer 3 56
98 TPS59640EVM-751 Internal Layer 4 56
99 TPS59640EVM-751 Internal Layer 5 57
100 TPS59640EVM-751 Internal Layer 6 57
101 TPS59640EVM-751 Internal Layer 7 58

Copyright © 2012, Texas Instruments Incorporated

List of Tables

1 TPS59640EVM-751 Electrical Performance Specifications 6
2 Current Limit Trip Selection 24
3 CPU Frequency Selection 25
4 GPU Frequency Selection 25
5 GPU Overshoot/Undershoot Reduction Selection 25
6 GPU Overshoot/Undershoot Reduction Selection 26
7 F2806 DSP Program Mode Selection 26
8 F2806 DSP Program Mode Selection 26
9 Onboard Dynamic Load Selection 26
10 VR_ON Enable Selection 27
11 VDDQ S3, S5 Enable Selection 27
12 VCCIO Output Voltage Selection 27
13 Bill of Materials 59

1 Description

The TPS59640EVM-751 evaluation module is designed to use a 9-V to 20-V input bus to produce six regulated outputs for the IMVP-7 SVID CPU/GPU Power System. The TPS59640EVM-751 is specially designed to demonstrate the TPS59640 full IMVP-7 mobile feature while providing a GUI communication program and a number of test points to evaluate the static and dynamic performance of the TPS59640.

1.1 Typical Applications

- IMVP-7 Vcore applications for adapter, battery, NVDC, or 3-V/5-V/12-V rails

1.2 Features

The TPS59640EVM-751 features:

- Complete solution for 9-V to 20-V input Intel IMVP-7 SVID Power System
- GUI communication to demonstrate full IMVP-7 mobile feature
- Three-phase CPU Vcore can support up to 94-A output current
- One-Phase GPU Vcore can support up to 33-A output current
- Eight selectable switching frequencies for CPU and GPU power
- Eight levels selectable current limit for CPU and GPU power
- Eight levels selectable output overshoot/undershoot reduction (**OSR/USR**™) for CPU and GPU power
- Switches or jumpers for each output enable
- Onboard dynamic load for CPU, GPU Vcore and VCCIO output
- High efficiency and high density by using TI power block MOSFET
- Convenient test points for probing critical waveforms
- Eight-layer PCB with 2-oz copper

Copyright © 2012, Texas Instruments Incorporated

2 TPS59640EVM-751 Power System Block Diagram

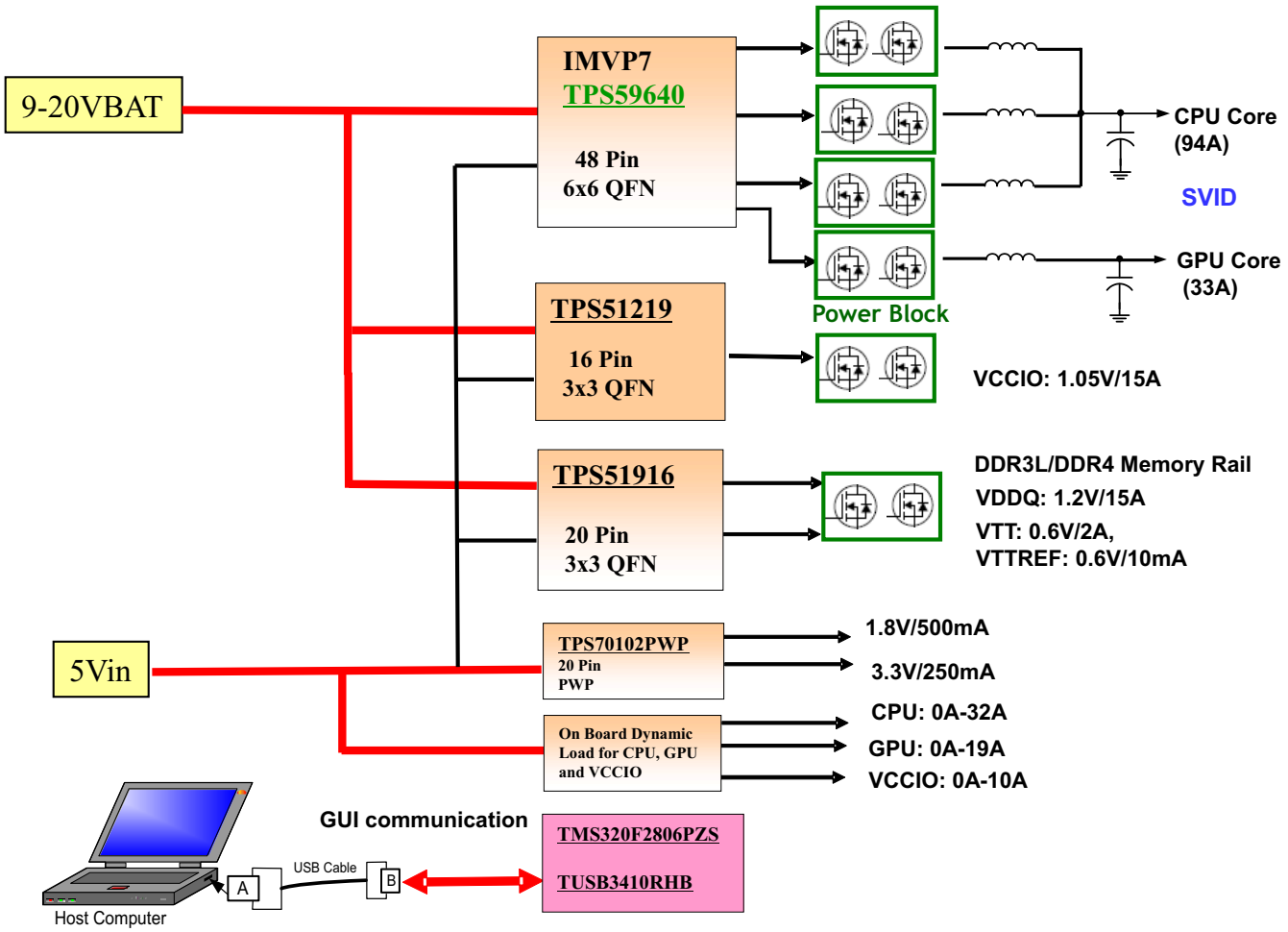


Figure 1. TPS59640EVM-751 Power System Block Diagram

Copyright © 2012, Texas Instruments Incorporated

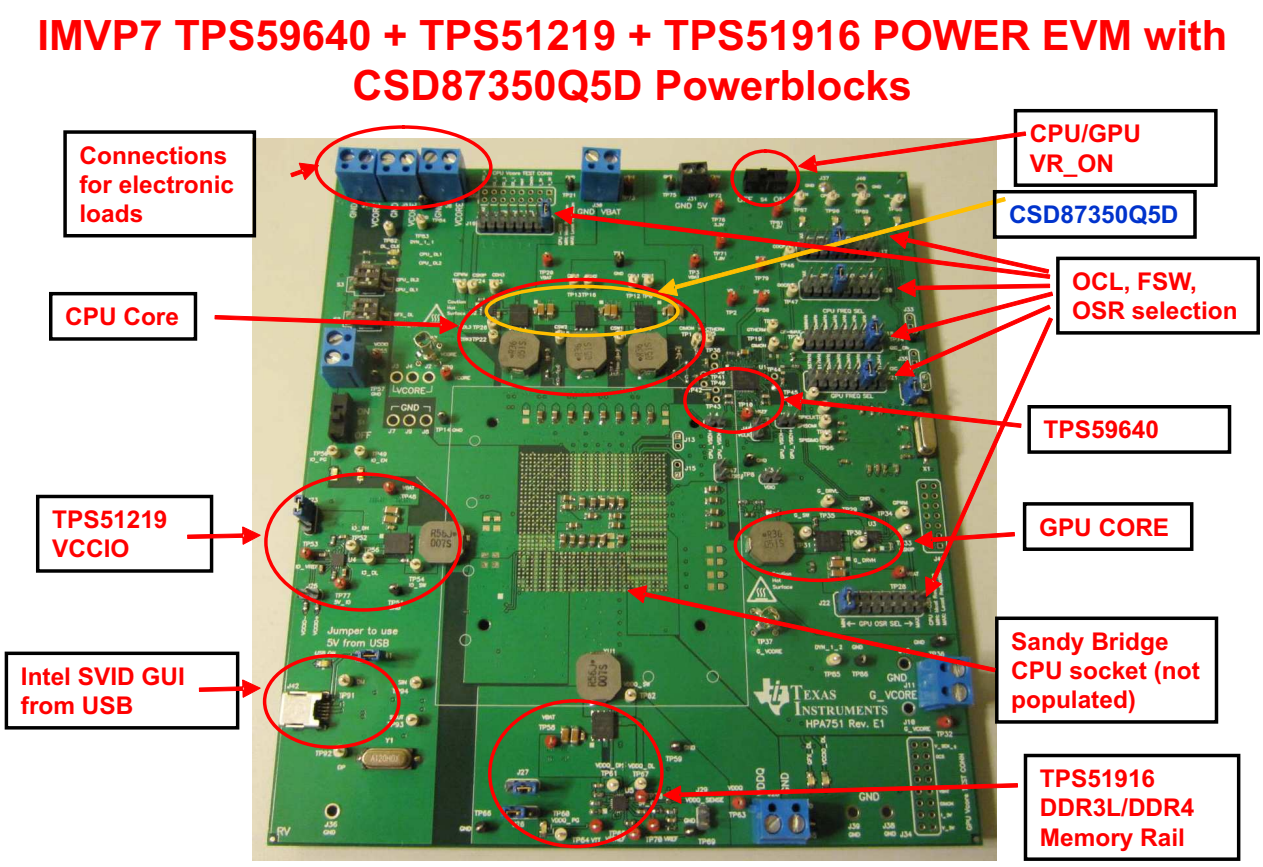


Figure 2. TPS59640EVM-751 EVM Illustration

3 Electrical Performance Specifications

Table 1. TPS59640EVM-751 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
12VBAT input voltage range	VBAT	9	12	20	V
Maximum input current	VBAT = 12 V, all full load (3-Phase CPU/1-Phase GPU)		16.2		A
No-load input current	VBAT=12 V, all no load(3-Phase CPU/1-Phase GPU)		0.1		A
5VIN input voltage range	Vin = 5 V	4.5	5	5.5	V
Maximum input current	VBAT =12 V, all full load		0.3		A
No-load input current	VBAT=12 V, all no load		0.1		A
OUTPUT CHARACTERISTICS					
CPU (TPS59640)					
Output voltage Vcore	SVID: address:00 CPU, payload: 1.05 V		1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation(droop) load line		–1.9		mΩ
Output voltage ripple	VBAT=12 V, 1.05 V/90 A (3-Phase) at 300 kHz		25		mVpp
Output load current	CPU 3-Phase operation	0		94	A
Output over current	Selectable per phase		37		A
Switching frequency	Selectable	250	300	600	kHz
Full load efficiency	VBAT=12 V, 1.05 V/94 A at 300 kHz		80.05%		

Copyright © 2012, Texas Instruments Incorporated

Table 1. TPS59640EVM-751 Electrical Performance Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPU (TPS59640)					
Output voltage Vcore	SVID: address:01 GPU, payload: 1.23 V		1.23		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation (droop) load line		–3.9		mΩ
Output voltage ripple	VBAT = 12 V, 1.23 V/35 A at 385 kHz		30		mVpp
Output load current	CPU 3-Phase operation	0		35	A
Output over current	Selectable per phase		37		A
Switching frequency	Selectable	275	385	660	kHz
Full load efficiency	VBAT = 12 V, 1.23 V/35 A at 385 kHz		81.99%		
1.05-V VCCIO (TPS51219)					
Output voltage			1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		0.1%		
Output voltage ripple	VBAT =12 V, 1.05 V/15 A		30		mVpp
Output load current		0		15	A
Output over current			24		A
Switching frequency	Selectable		500		kHz
Full load efficiency	VBAT = 12 V, 1.05 V/15 A		89.27%		
DDR3L/DDR4 MEMORY RAIL (TPS51916)					
Output voltage			1.2		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		0.1%		
Output voltage ripple	VBAT = 12 V, 1.2 V/15 A		30		mVpp
Output load current		0		15	A
Output over current			24		A
Switching frequency	Selectable		500		kHz
Full-load efficiency	VBAT = 12 V, 1.2 V/15 A		90.62%		
Operating temperature			25		°C

Copyright © 2012, Texas Instruments Incorporated

Note: Jumpers set to default locations; see Section 6 of this user's guide.

4 Schematic

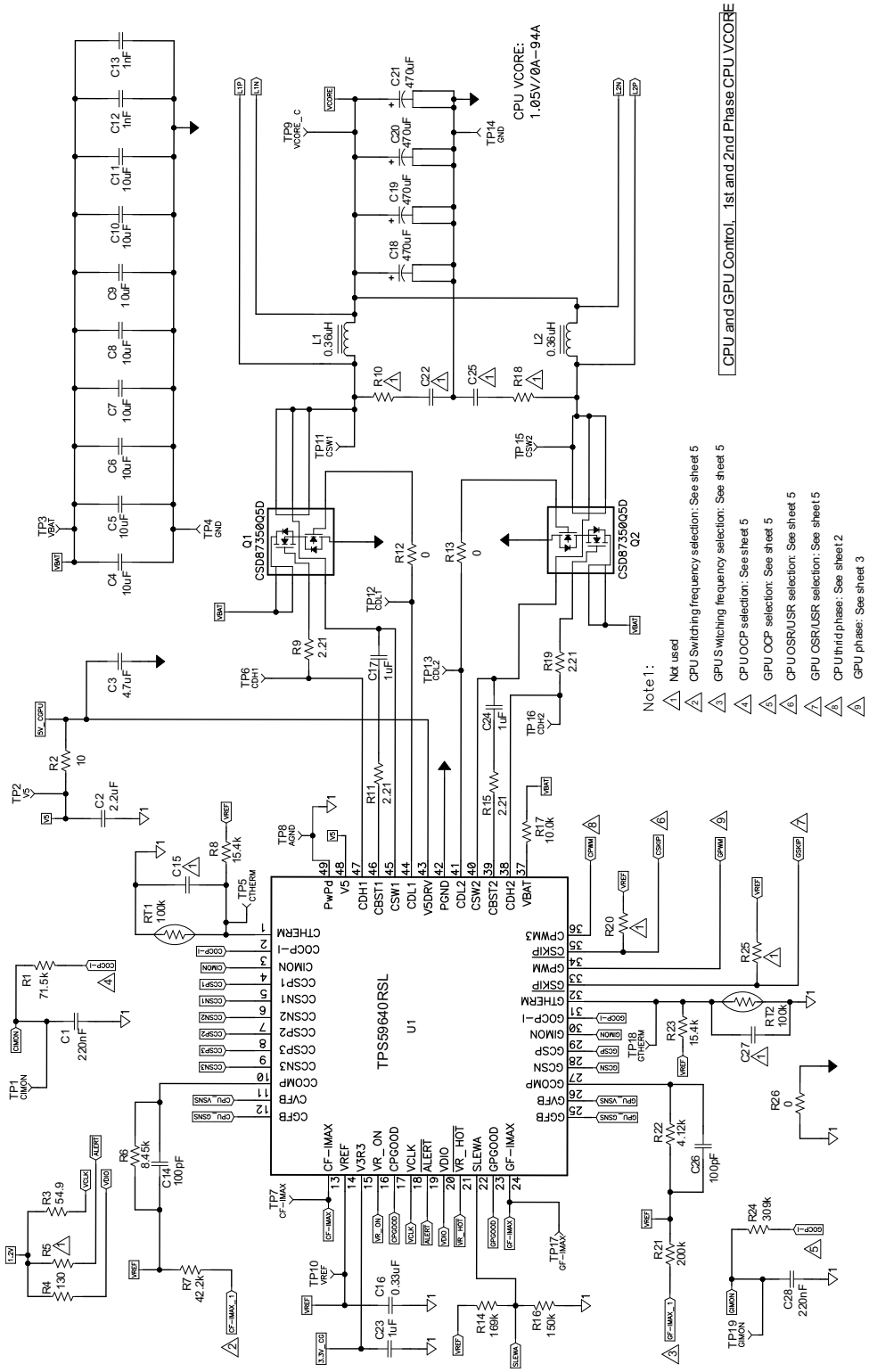


Figure 3. TPS59640EVM-751 Schematic (1 of 13)

Copyright © 2012, Texas Instruments Incorporated

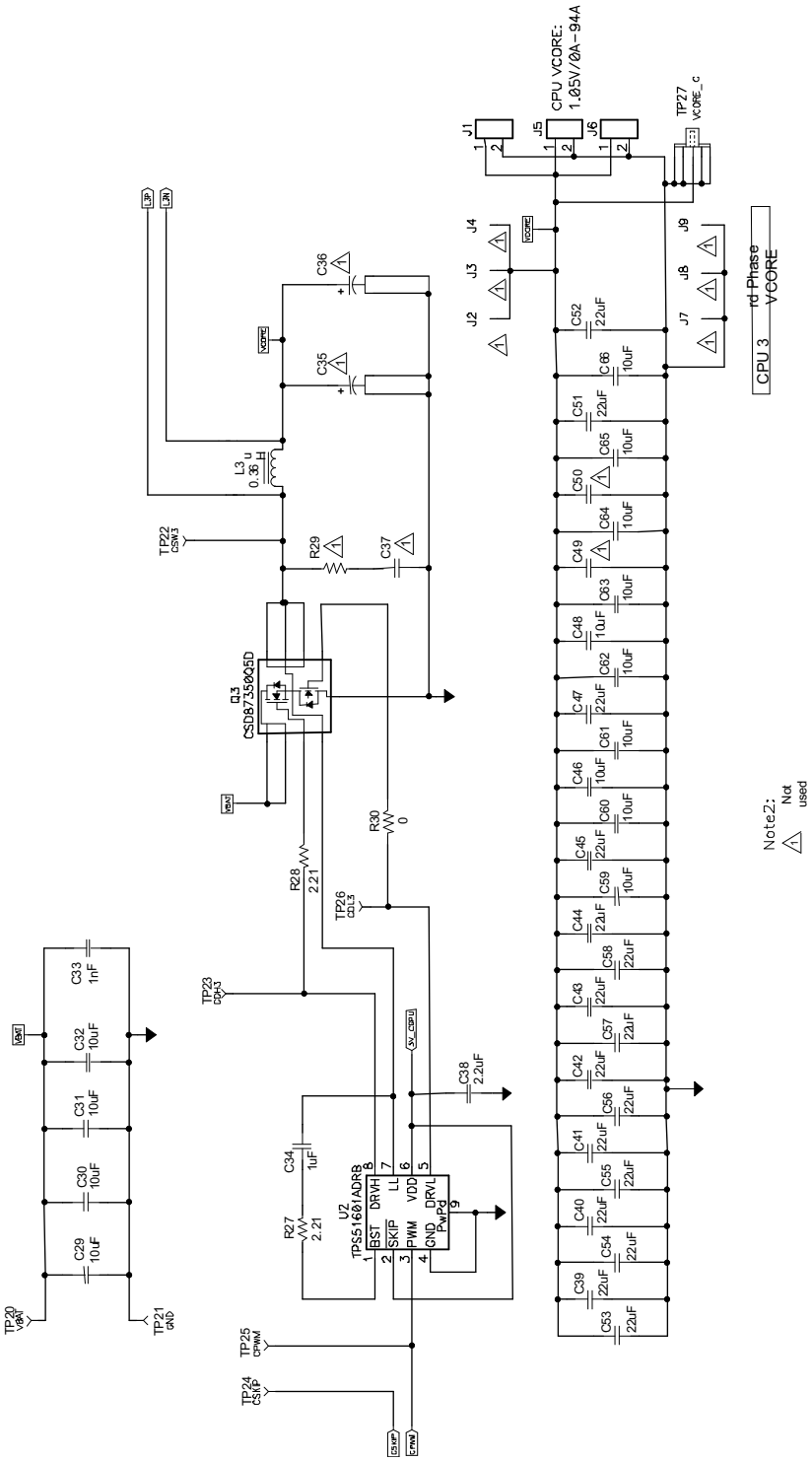


Figure 4. TPS59640EVM-751 Schematic (2 of 13)

Copyright © 2012, Texas Instruments Incorporated

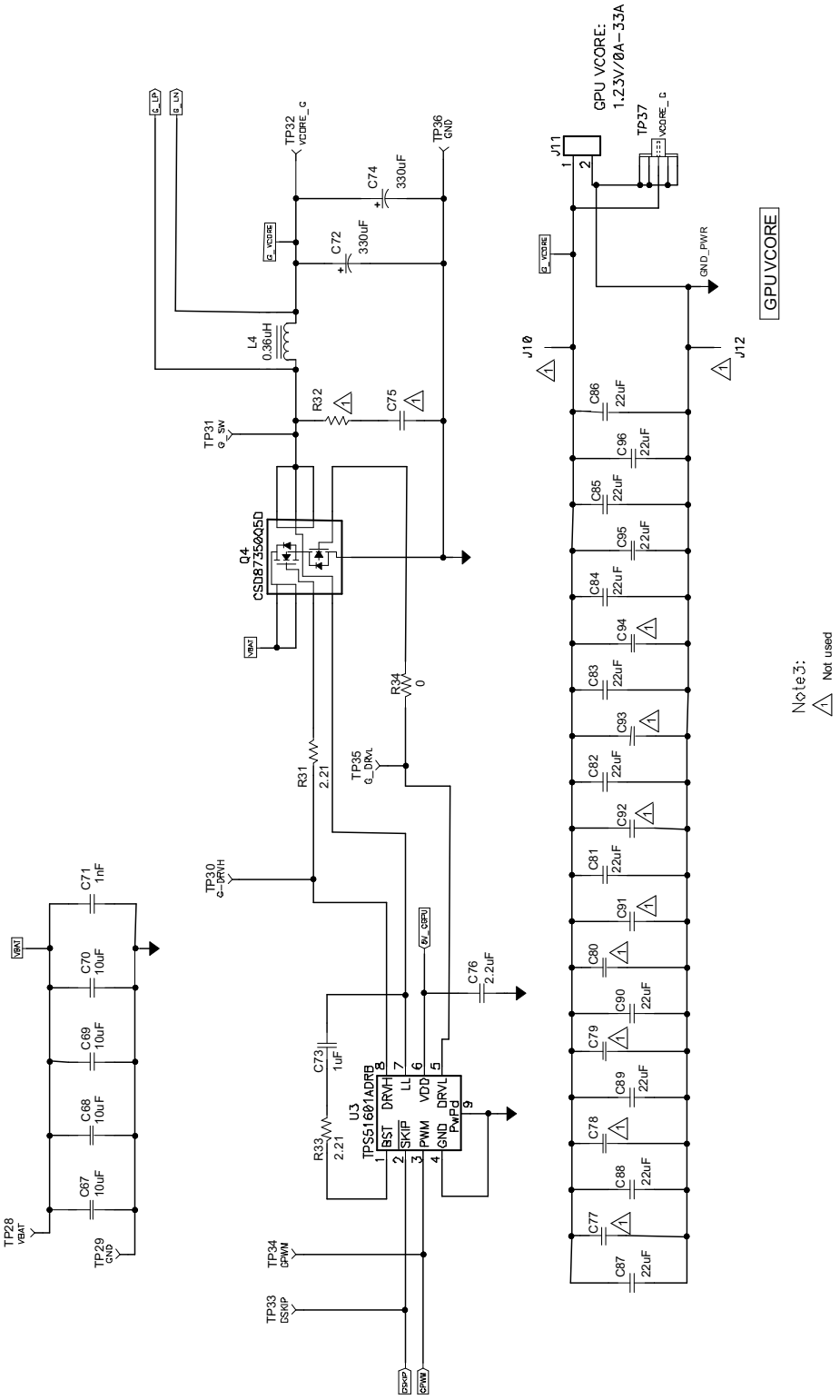


Figure 5. TPS59640EVM-751 Schematic (3 of 13)

Copyright © 2012, Texas Instruments Incorporated

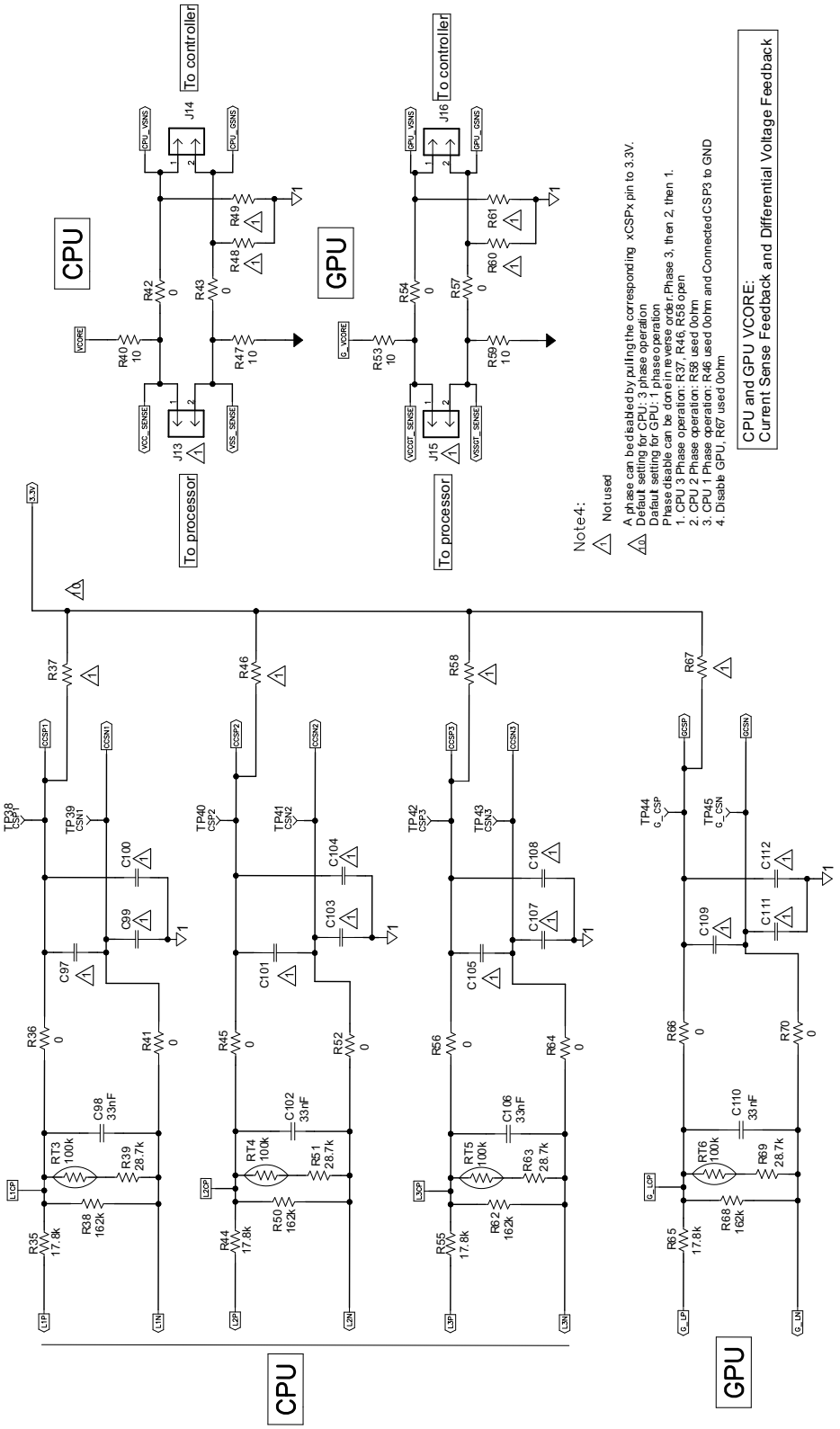


Figure 6. TPS59640EVM-751 Schematic (4 of 13)

Copyright © 2012, Texas Instruments Incorporated

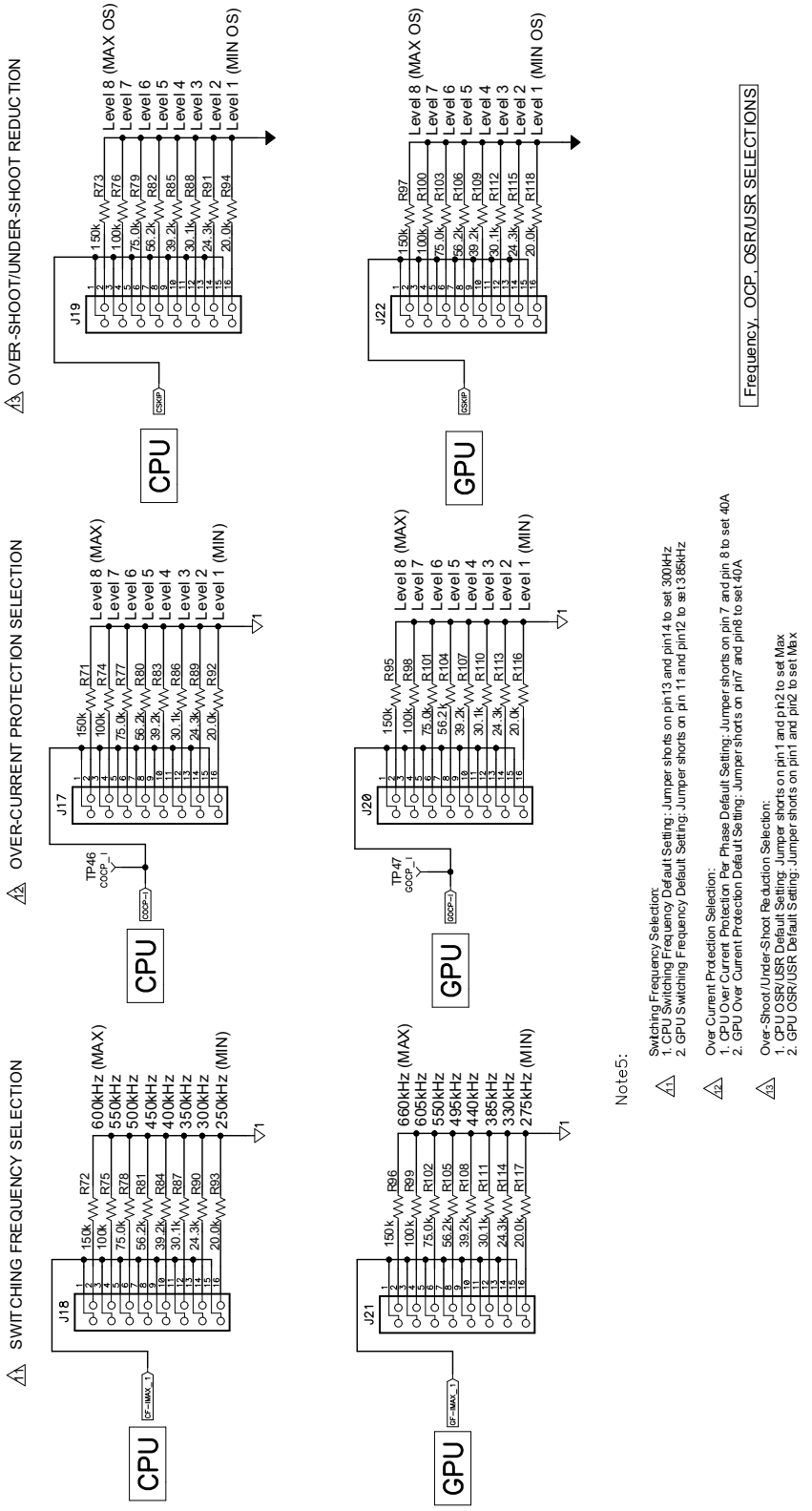


Figure 7. TPS59640EVM-751 Schematic (5 of 13)

Copyright © 2012, Texas Instruments Incorporated

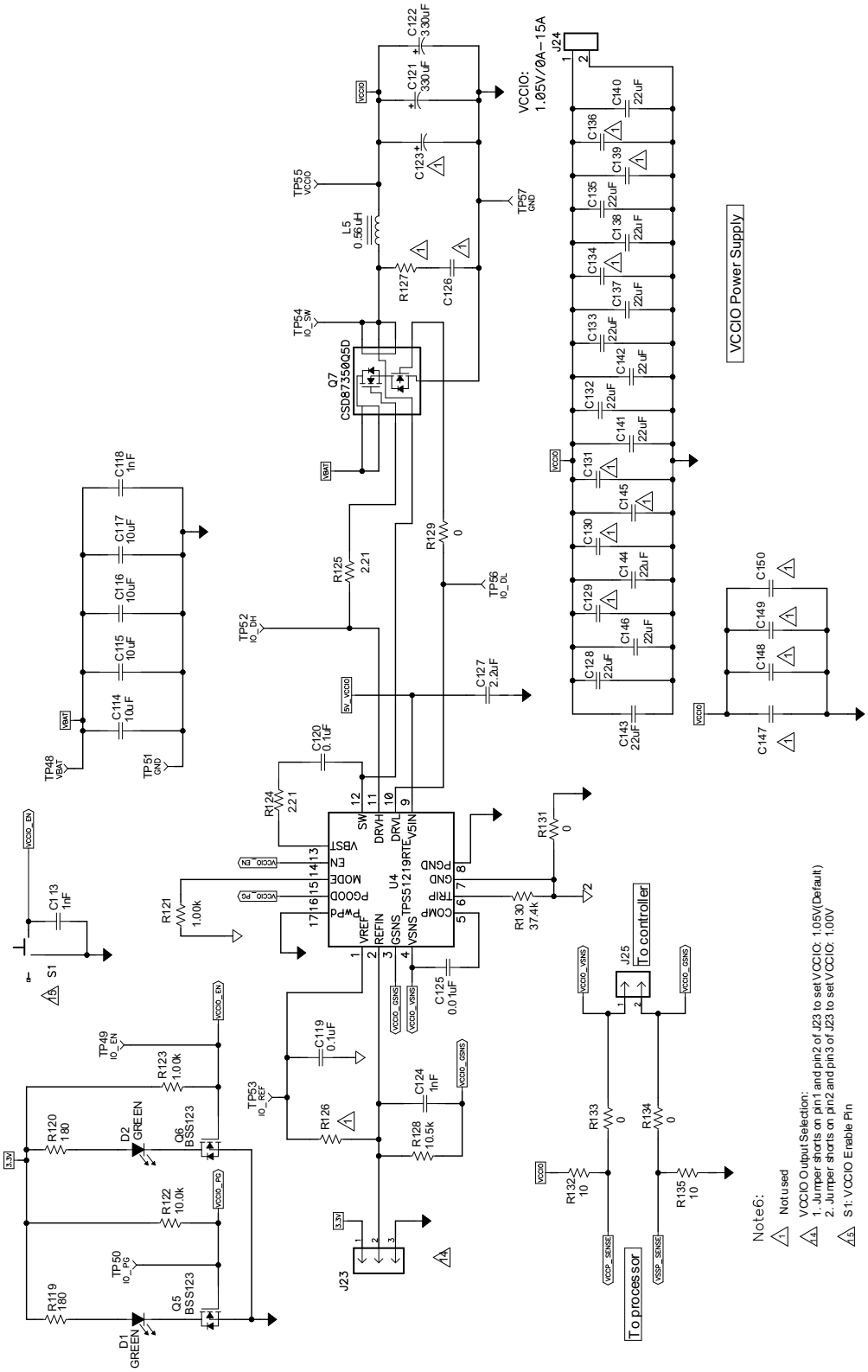


Figure 8. TPS59640EVM-751 Schematic (6 of 13)

Copyright © 2012, Texas Instruments Incorporated

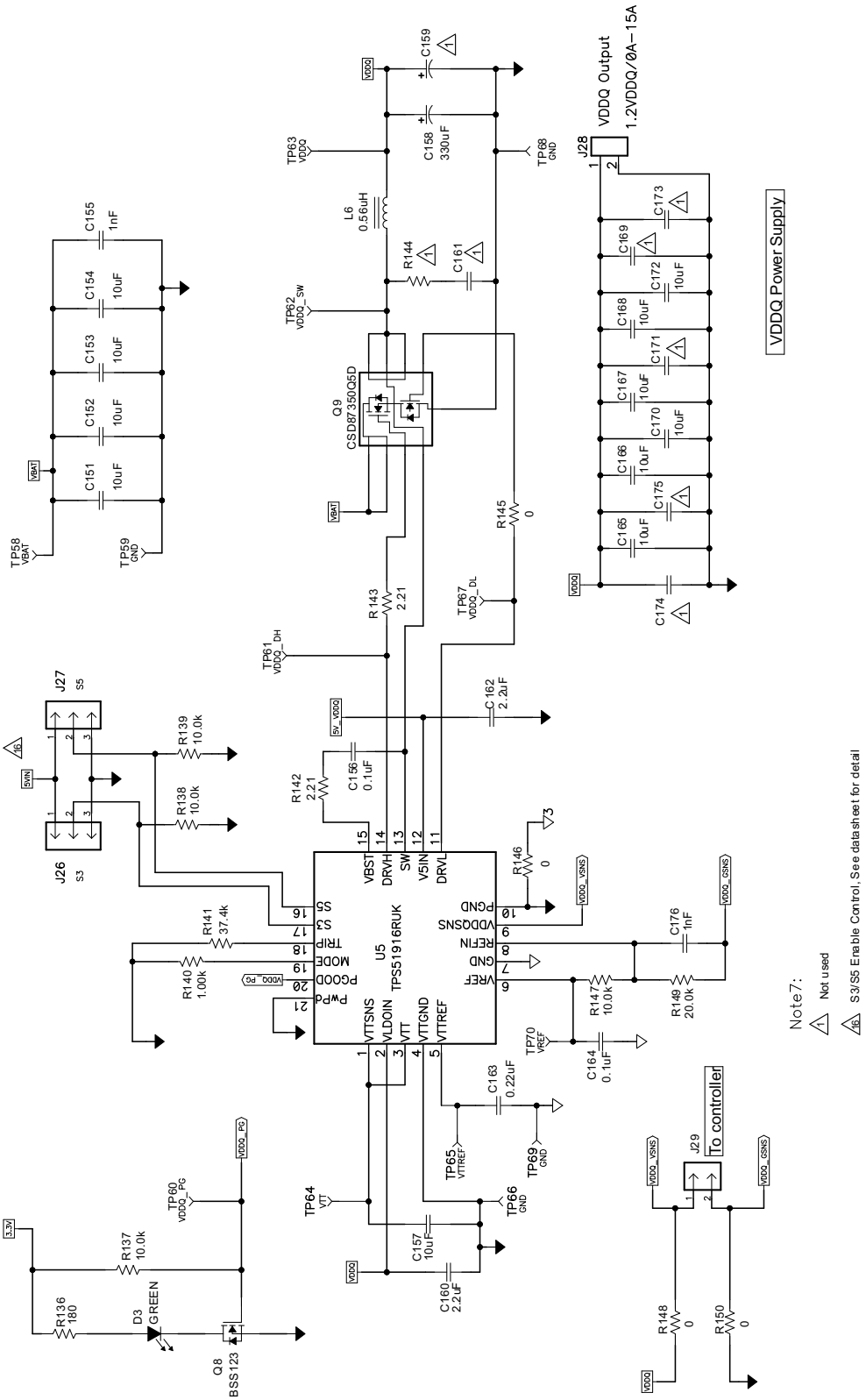


Figure 9. TPS59640EVM-751 Schematic (7 of 13)

Copyright © 2012, Texas Instruments Incorporated

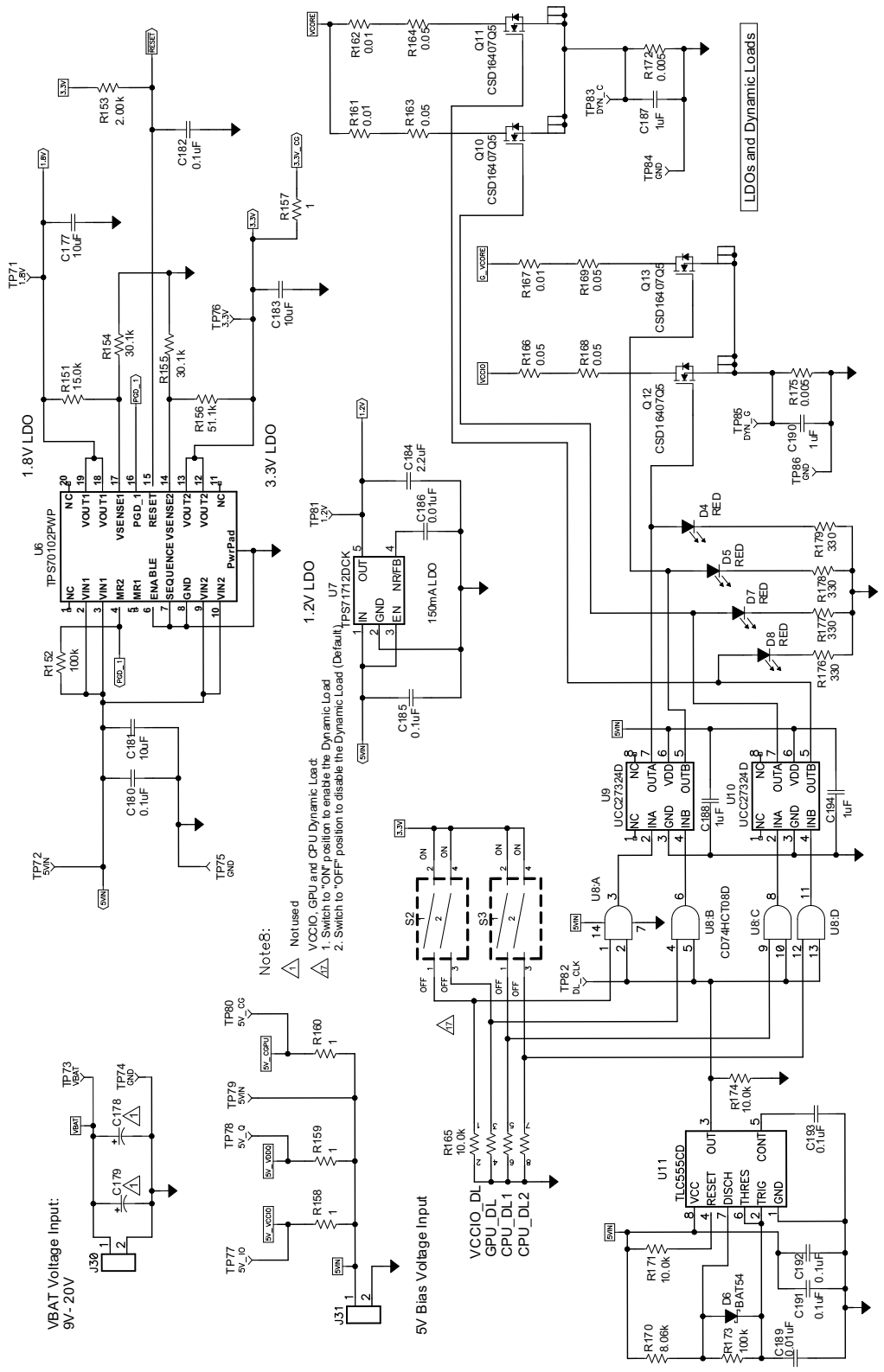


Figure 10. TPS59640EVM-751 Schematic (8 of 13)

Copyright © 2012, Texas Instruments Incorporated

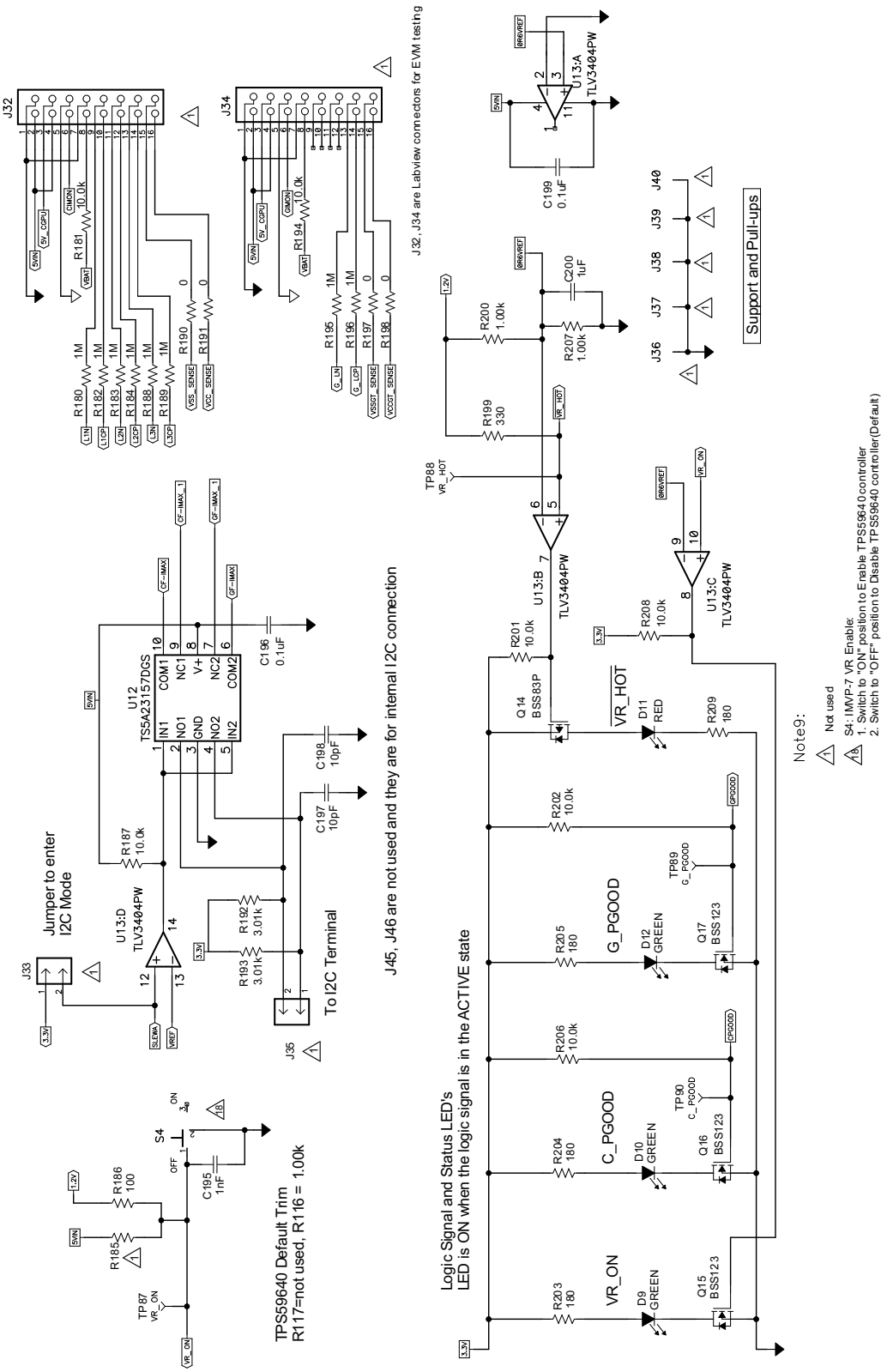


Figure 11. TPS59640EVM-751 Schematic (9 of 13)

Copyright © 2012, Texas Instruments Incorporated

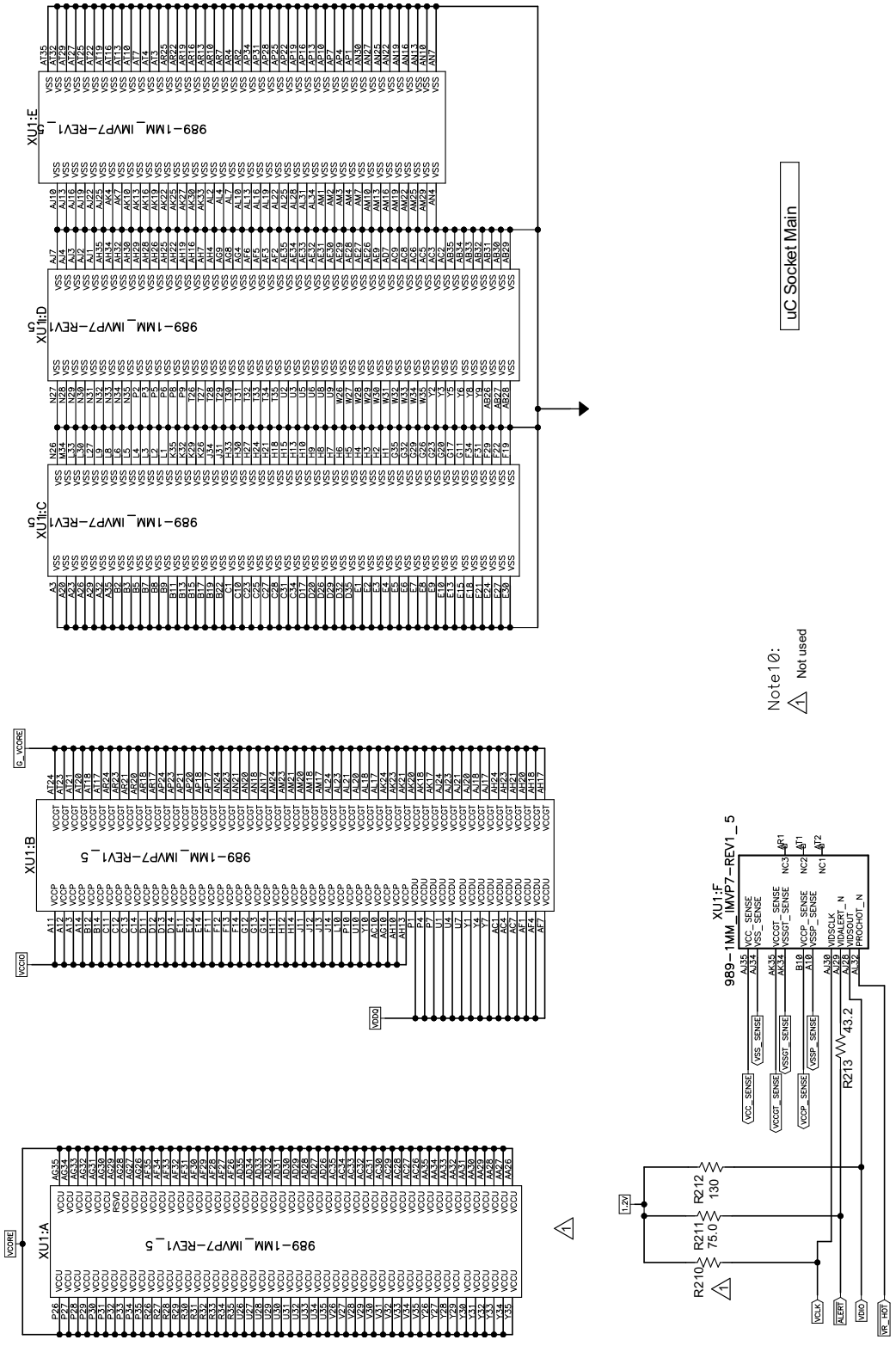


Figure 12. TPS59640EVM-751 Schematic (10 of 13)

Copyright © 2012, Texas Instruments Incorporated

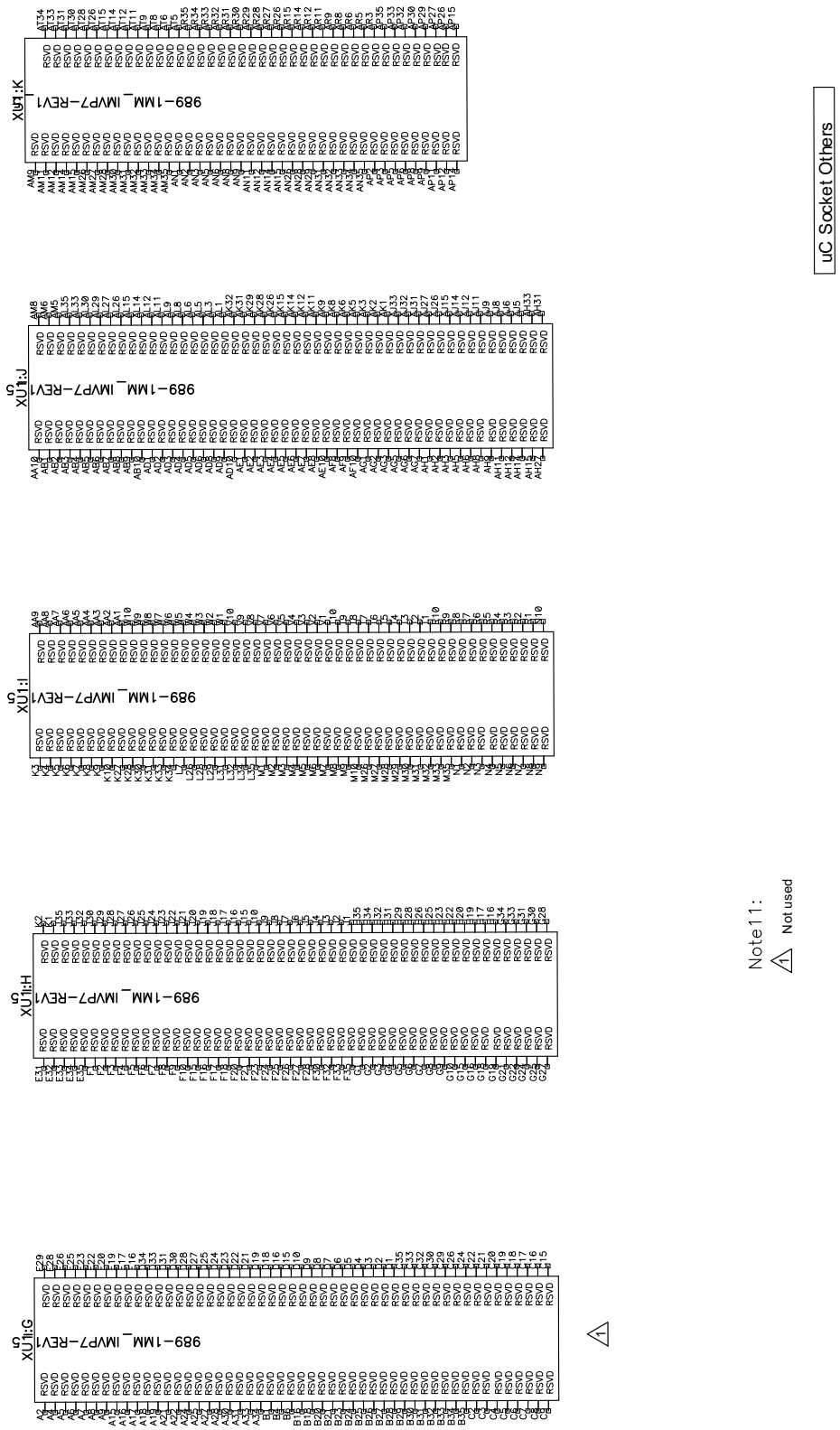


Figure 13. TPS59640EVM-751 Schematic (11 of 13)

Copyright © 2012, Texas Instruments Incorporated

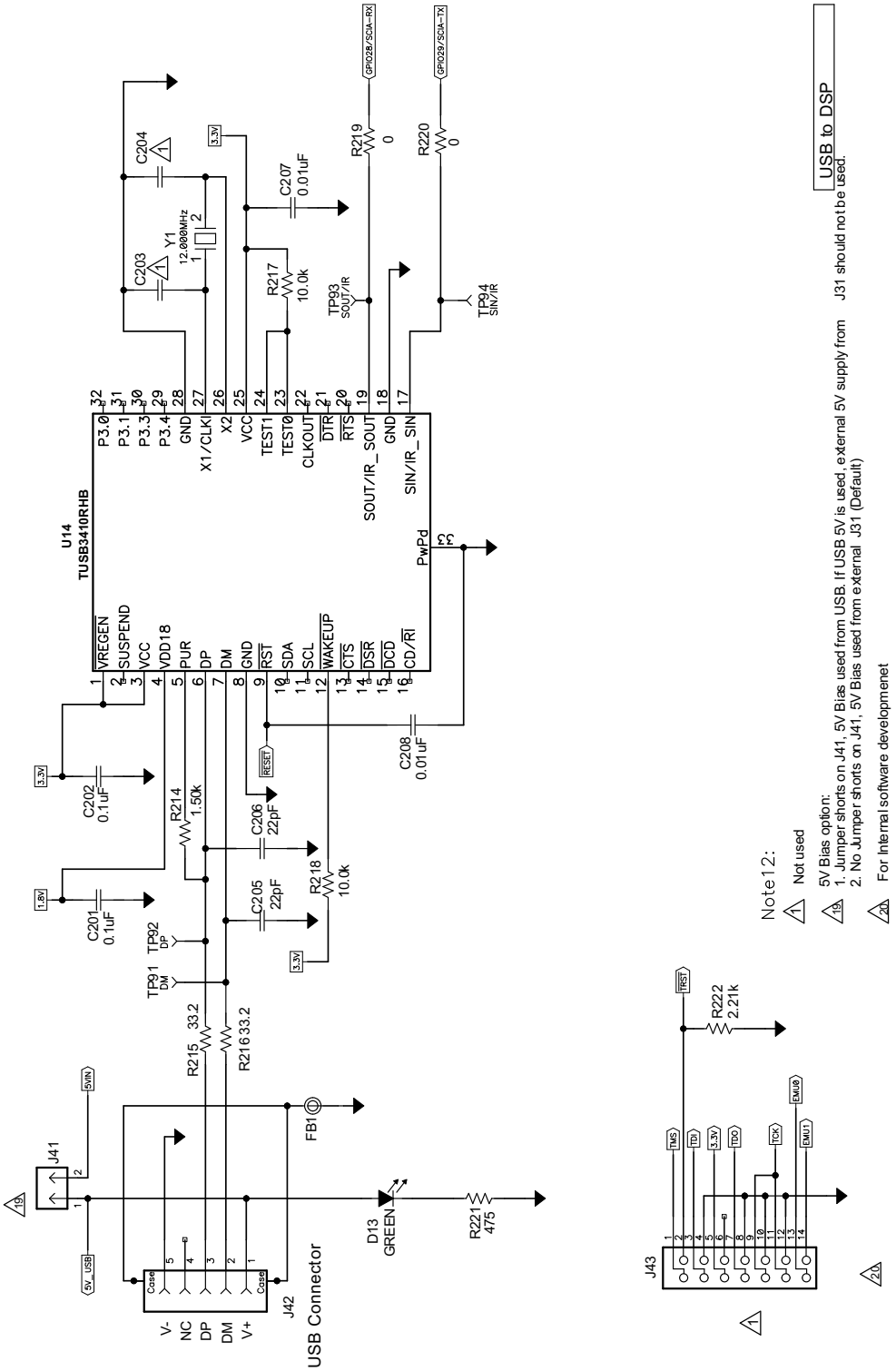


Figure 14. TPS59640EVM-751 Schematic (12 of 13)

Copyright © 2012, Texas Instruments Incorporated

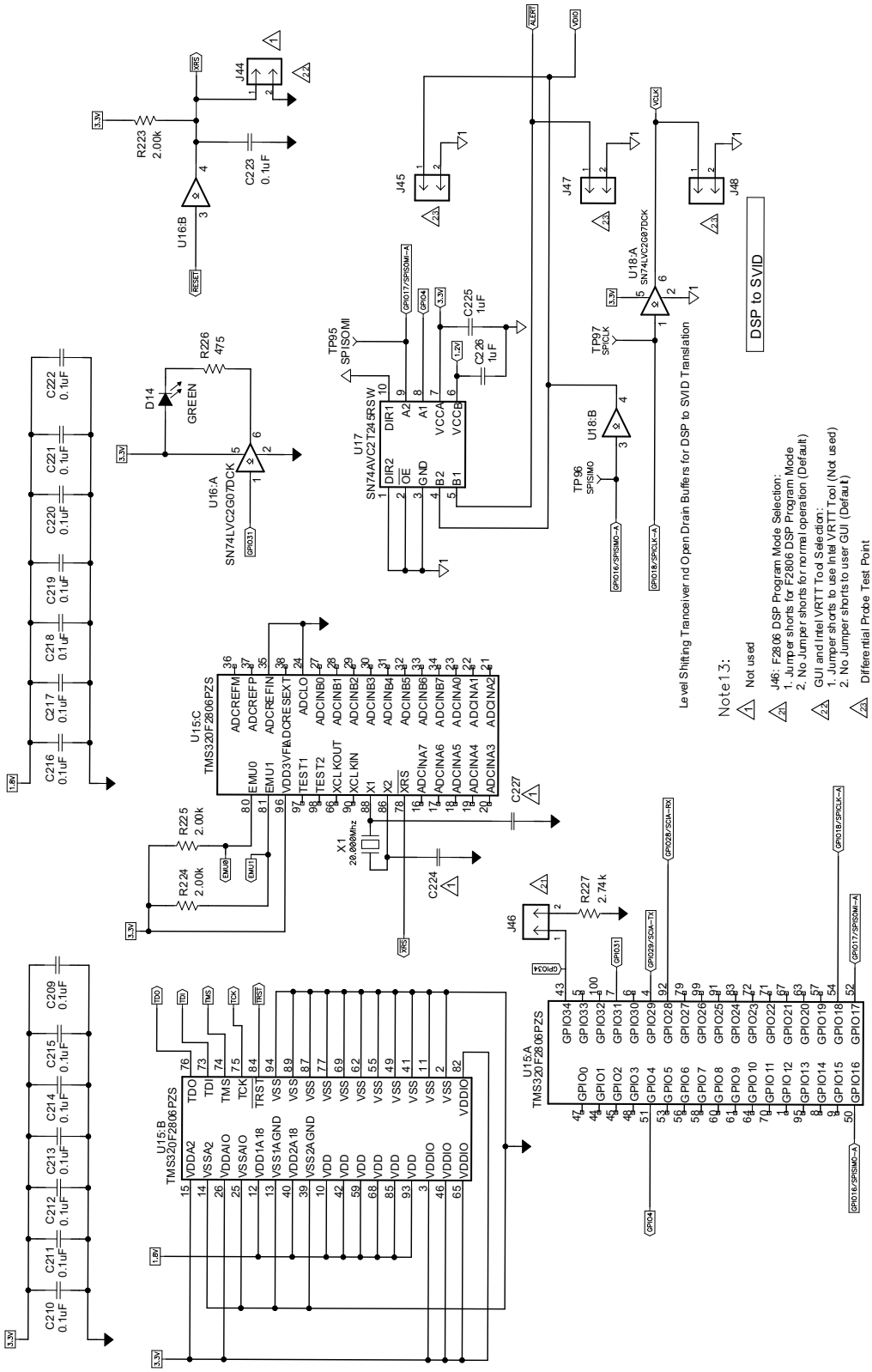


Figure 15. TPS59640EVM-751 Schematic (13 of 13)

Copyright © 2012, Texas Instruments Incorporated

5 Test Setup

5.1 Test Equipment

5.1.1 Personal Computer (Host Computer)

Microsoft Windows™ XP or newer with available USB port

5.1.2 USB Cable

The USB cable: standard USB_A to USB_B, 5-pin, mini-B cable. See the Figure 16 illustration.



Figure 16. USB Cable

5.1.3 TPS59640 USB Driver and SVID GUI Installation

1. Copy the file *swrc094f.zip* to the host computer.
2. Copy the file *TI-SVID-GUI_1_5_0_1 exe* to the host computer.
3. Extract *setup.exe* from the aforementioned .zip file.
4. Double-click on this setup.exe. This loads the TUSB drivers files to the host computer on C:\Program Files\Texas Instruments Inc\TUSB3410 Single Driver installer\DISK1
5. Then, go to this location on the host computer (C:\Program Files\Texas Instruments Inc\TUSB3410 Single Driver installer\DISK1), and double-click *setup.exe*. This installs the TUSB driver.

5.1.4 DC Source

12VBAT DC Source: The 12VBAT DC source must be a 0-V to 20-V variable DC source capable of supplying a 20-Adc current. Connect 12VBAT to J30 as shown in Figure 17.

5Vin DC Source: The 5Vin DC source must be a 0-V to 5-V variable DC source capable of supplying a 1-Adc current. Connect 5Vin to J31 as shown in Figure 17.

5.1.5 Meters

- V1: 5Vin at TP72(5Vin) and TP75 (GND)
- V2: 12VBAT at TP73(VBAT) and TP21 (GND)
- V3: CPU Vcore sense voltage at J14; GPU Vcore sense voltage at J16; VDDQ sense voltage at J29, VCCIO sense voltage at J25
- A1: 12VBAT input current

5.1.6 Load

The output load must be an electronic constant current load capable of 0 Adc to 90 Adc.

Copyright © 2012, Texas Instruments Incorporated

5.1.7 Oscilloscope

A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for 1-MΩ impedance, 20-MHz bandwidth, AC coupling, 2-µs/division horizontal resolution, 50-mV/division vertical resolution. Test points TP27 and TP37 can be used to measure the output ripple voltage for CPU and GPU. Do not use a leaded ground connection as this can induce additional noise due to the large ground loop.

5.2 Recommended Wire Gage

1. **V5in to J31 (5-V input):**
   The recommended wire size is 1 x AWG 18 per input connection, with the total length of wire less than 4 feet (2- foot input, 2-foot return).
2. **12VBAT to J30 (12-V input):**
   The recommended wire size is 1 x AWG 16 per input connection, with the total length of wire less than 4 feet (2-foot input, 2-foot return).
3. **J1, J5, J6 (CPU) to LOAD or J11 (GPU) to LOAD or J28 (VDDQ) to LOAD or J24 (VCCIO) to LOAD**
   The minimum recommended wire size is 2 x AWG 16, with the total length of wire less than 4 feet (2-foot output, 2-foot return)

5.3 Recommended Test Setup

Figure 17 is the recommended test setup to evaluate the TPS59640EVM-751. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before handling the EVM.

Copyright © 2012, Texas Instruments Incorporated

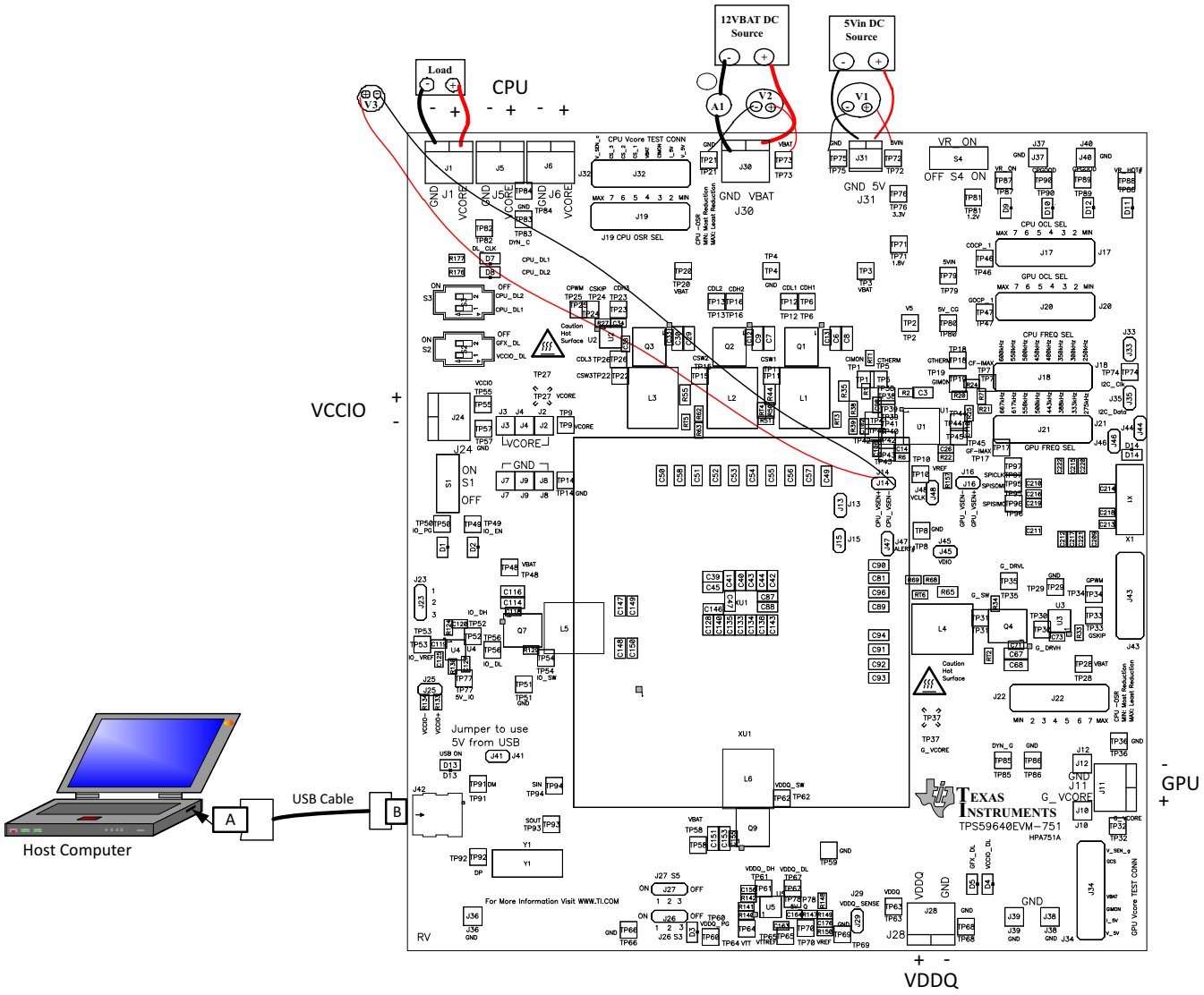


Figure 17. TPS59640EVM-751 Recommended Test Setup

5.4 USB Cable Connections

A standard USB_A and 5-pin mini_B USB cable is required to connect the host computer to J42 USB port (left bottom side). A green LED (D13) lights up near the USB port on the EVM. This indicates that the USB cable is connected.

5.5 Input Connections

1. Prior to connecting the 5Vin DC source, it is advisable to limit the source current from 5 Vin to 1 A maximum. Make sure that 5Vin is initially set to 0 V and connected as shown in Figure 17.
2. Prior to connecting the 12VBAT DC source, it is advisable to limit the source current from 12VBAT to 10 A maximum. Make sure that 12VBAT is initially set to 0 V and connected as shown in Figure 17.
3. Connect voltmeters V1 at TP72 (5Vin) and TP75 (GND) to measure 5Vin voltage, V2 at TP73 (12 VBAT), and TP21 (GND) to measure 12VBAT voltage as shown in Figure 17.
4. Connect a current meter A1 between 12VBAT DC source and J30 to measure the 12VBAT input current.

Copyright © 2012, Texas Instruments Incorporated

5.6 Output Connections

1. Connect the load to J1, J5, and J6, and set the load to constant resistance mode to sink 0 Adc before 5Vin and 12VBAT are applied. This is for CPU operation.
2. Connect a voltmeter V3 at J14 to measure CPU Vcore sense voltage.

6 Configuration

All jumper selections must be made prior to applying power to the EVM. The user can configure this EVM per the following configurations.

6.1 CPU and GPU Configuration

6.1.1 CPU/GPU Current Limit Trip Selection (J17 for CPU and J20 for GPU)

The current limit trip can be set by J17 (COCP) and J20 (GOCP).

Default setting: Level 5 for both CPU and GPU.

Table 2. Current Limit Trip Selection

Jumper Set to	Connected Resistor	COCP Limit (Typ)
Left (1-2 pin shorted)	150k	Max
Second (3-4 pin shorted)	100k	Level 7
Third (5-6 pin shorted)	75k	Level 6
Fourth (7-8 pin shorted)	**56.2k**	**Level 5**
Fifth (9-10 pin shorted)	39.2k	Level 4
Sixth (11-12 pin shorted)	30.1k	Level 3
Seventh (13-14 pin shorted)	24.3k	Level 2
Right (15-16 pin shorted)	20.0k	Min

Copyright © 2012, Texas Instruments Incorporated

6.1.2 CPU Frequency Selection (J18)

The operating frequency can be set by J18

Default setting: 300 kHz for CPU.

Table 3. CPU Frequency Selection

Jumper Set to	Connected Resistor	CPU
Left (1-2 pin shorted)	150k	600 kHz
Second (3-4 pin shorted)	100k	550 kHz
Third (5-6 pin shorted)	75k	500 kHz
Fourth (7-8 pin shorted)	56.2k	450kHz
Fifth (9-10 pin shorted)	39.2k	400kHz
Sixth (11-12 pin shorted)	30.1k	350kHz
Seventh (13-14 pin shorted)	**24.3k**	**300kHz**
Right(15-16 pin shorted)	20.0k	250kHz

6.1.3 GPU Frequency Selection (J21)

The operating frequency can be set by J21.

Default setting: 385 kHz for GPU.

Table 4. GPU Frequency Selection

Jumper Set to	Connected Resistor	CPU
Left (1-2 pin shorted)	150k	660kHz
Second (3-4 pin shorted)	100k	605kHz
Third (5-6 pin shorted)	75k	550kHz
Fourth (7-8 pin shorted)	56.2k	495kHz
Fifth (9-10 pin shorted)	39.2k	440kHz
Sixth (11-12 pin shorted)	**30.1k**	**385kHz**
Seventh (13-14 pin shorted)	24.3k	330kHz
Right(15-16 pin shorted)	20.0k	275kHz

6.1.4 CPU Overshoot/Undershoot Reduction Selection (J19)

The overshoot/undershoot reduction can be set by J19 CSKIP.

Default setting: Max.

Table 5. GPU Overshoot/Undershoot Reduction Selection

Jumper Set to	Connected Resistor	CPU
Left (1-2 pin shorted)	**150k**	**Max**
Second (3-4 pin shorted)	100k	Level 7
Third (5-6 pin shorted)	75k	Level 6
Fourth (7-8 pin shorted)	56.2k	Level 5
Fifth (9-10 pin shorted)	39.2k	Level 4
Sixth (11-12 pin shorted)	30.1k	Level 3
Seventh (13-14 pin shorted)	24.3k	Level 2
Right(15-16 pin shorted)	20.0k	Min

Copyright © 2012, Texas Instruments Incorporated

6.1.5 GPU Overshoot/Undershoot Reduction Selection (J22)

The overshoot/undershoot reduction can be set by J22 GSKIP.

Default setting: Max.

Table 6. GPU Overshoot/Undershoot Reduction Selection

Jumper Set to	Connected Resistor	CPU
Right (1-2 pin shorted)	**150k**	**Max**
Second (3-4 pin shorted)	100k	Level 7
Third (5-6 pin shorted)	75k	Level 6
Fourth (7-8 pin shorted)	56.2k	**Level 5**
Fifth (9-10 pin shorted)	39.2k	Level 4
Sixth (11-12 pin shorted)	30.1k	Level 3
Seventh (13-14 pin shorted)	24.3k	Level 2
Left(15-16 pin shorted)	20.0k	Min

6.1.6 F2806 DSP Program Mode Selection (J46)

The F2806 DSP Program Mode (GUI) Selection can be set by J46.

Default setting: No jumper shorts on J46 for normal operation

Table 7. F2806 DSP Program Mode Selection

Jumper Set to	Program Mode Selection
No jumper on J46	**Normal operation**
Jumper on J46	Flash the DSP program to the EVM

6.1.7 5Vin Bias Voltage Option (J41)

The 5-Vin bias voltage can be used from USB or externally.

Default setting: No jumper shorts on J41

Table 8. F2806 DSP Program Mode Selection

Jumper Set to	Program Mode Selection
No jumper	**5-Vin Bias from J31 external**
Jumper shorted	5-Vin Bias from USB, 5 Vin from J31 must not be connected

6.1.8 Onboard Dynamic Load Selection [S3 for CPU, S2 [Upper) for GPU, S2 (Lower) for VCCIO]

The onboard dynamic load can be set by S2 and S3.

Default setting: Push S2 and S3 to *OFF* position to disable the on board dynamic load.

Table 9. Onboard Dynamic Load Selection

Switch Set to	Dynamic Load Selection
Push S3 to *ON* position	Enable 32-A onboard dynamic load at CPU
Push S3 to *OFF* position	**Disable 32-A onboard dynamic load at CPU**
Push S2 (upper) to *ON* position	Enable 19-A onboard dynamic load at GPU
Push S2 (upper) to *OFF* position	**Disable 19-A onboard dynamic load at GPU**
Push S2 (lower) to *ON* position	Enable 10-A onboard dynamic load at VCCIO
Push S2 (lower) to *OFF* position	**Disable 10-A onboard dynamic load at VCCIO**

Copyright © 2012, Texas Instruments Incorporated

6.1.9 IMVP-7 VR_ON Enable Selection (S4)

The IMVP-7 CPU/GPU can be enabled and disabled by S4.

Default setting: Push S4 to *OFF* position to disable both CPU and GPU.

Table 10. VR_ON Enable Selection

Switch Set to	VR_ON Selection
Push S4 to *ON* position	Enable IMVP-7 CPU/GPU Vcore
Push S4 to *OFF* position	**Disable IMVP-7 CPU/GPU Vcore**

6.2 1.2VDDQ, 0.6V VTT and 0.6V VTTREF Configuration

6.2.1 VDDQ S3, S5 Enable Selection

The controller can be enabled and disabled by J26 and J27.

Default setting: Jumper shorts on Pin 2 and Pin 3 of J27,
Jumper shorts on Pin 2 and Pin 3 of J26

Table 11. VDDQ S3, S5 Enable Selection

State	J26 (S3) Set to	J27 (S5) Set to	VDDQ	VTTREF	VTT
S0	ON position	ON position	ON	ON	ON
S3	OFF position	ON position	ON	ON	OFF (High-Z)
S4/S5	**OFF position**	**OFF position**	**OFF (Discharge)**	**OFF (Discharge)**	**OFF (Discharge)**

6.3 1.05V VCCIO Configuration

6.3.1 1.05V Enable Selection (S1)

1.05V enable can be set by S1.
Default setting: Push S1 to OFF position

6.3.2 VCCIO Output Voltage Selection (J23)

The VCCIO output voltage can be selected by J23.
Default setting: Jumper shorts pin 1 and pin 2 of J23

Table 12. VCCIO Output Voltage Selection

Jumper Set to	Selection
Jumper shorts on pin 1 and pin 2	**VCCIO: 1.05 V**
Jumper shorts on pin 2 and pin 3	VCCIO: 1.00 V

Copyright © 2012, Texas Instruments Incorporated

7 Test Procedure

7.1 Line/Load Regulation and Efficiency Measurement Procedure

7.1.1 CPU

1. Set up EVM as described in Section 5.3, Section 5.4, Section 5.5, Section 5.6, and Figure 17.
2. Ensure no jumper shorts are on J46.
3. Ensure all other jumpers configuration settings in this section before 5Vin and 12VBAT are applied.
4. Ensure load is set to constant resistance mode and to sink 0 Adc.
5. Ensure S1 and S4 are in *OFF* position.
6. Add scope probe on the TP27 for CPU Vcore ripple measurement.
7. Ensure USB cable is connected between host computer and USB port (J42) on the EVM.
8. Increase 5Vin from 0 V to 5 V. Use V1 to measure 5Vin input voltage.
9. Increase 12VBAT from 0 V to 12 V. Use V2 to measure 12VBAT input voltage.
10. Double-click the TI-SVID-GUI_1_5_0_1.exe to launch the GUI program. The GUI window shown in Figure 18 appears.
11. Push S4 to *ON* position to enable the VR_ON of TPS59640. VR_ON LED lights up.
12. Now you are ready to send SVID commends. The GUI at start-up defaults:
    Address: 00 CPU, Commend: SetVIDslow, Payload: 1.05V
    (The user can select the SVID commend by using the pulldown menu.)
13. Click *send Commend*, and the CPU CPGOOD LED lights up. See the GUI window as shown in Figure 18.
14. Measure V3: CPU Vcore at J14 and A1: 12VBAT input current
15. Vary CPU LOAD from 0 Adc to 90 Adc. The CPU Vcore must remain in load line.
16. Vary 12VBAT from 9 V to 20 V. The CPU Vcore must remain in line regulation.
17. Push S4 to *OFF* position to disable CPU Vcore controller.
18. Decrease LOAD to 0 A, and disconnect the LOAD from terminal J1, J5, and J6.
19. Disconnect V3 from J14.
20. Disconnect scope probe from TP27.

Copyright © 2012, Texas Instruments Incorporated

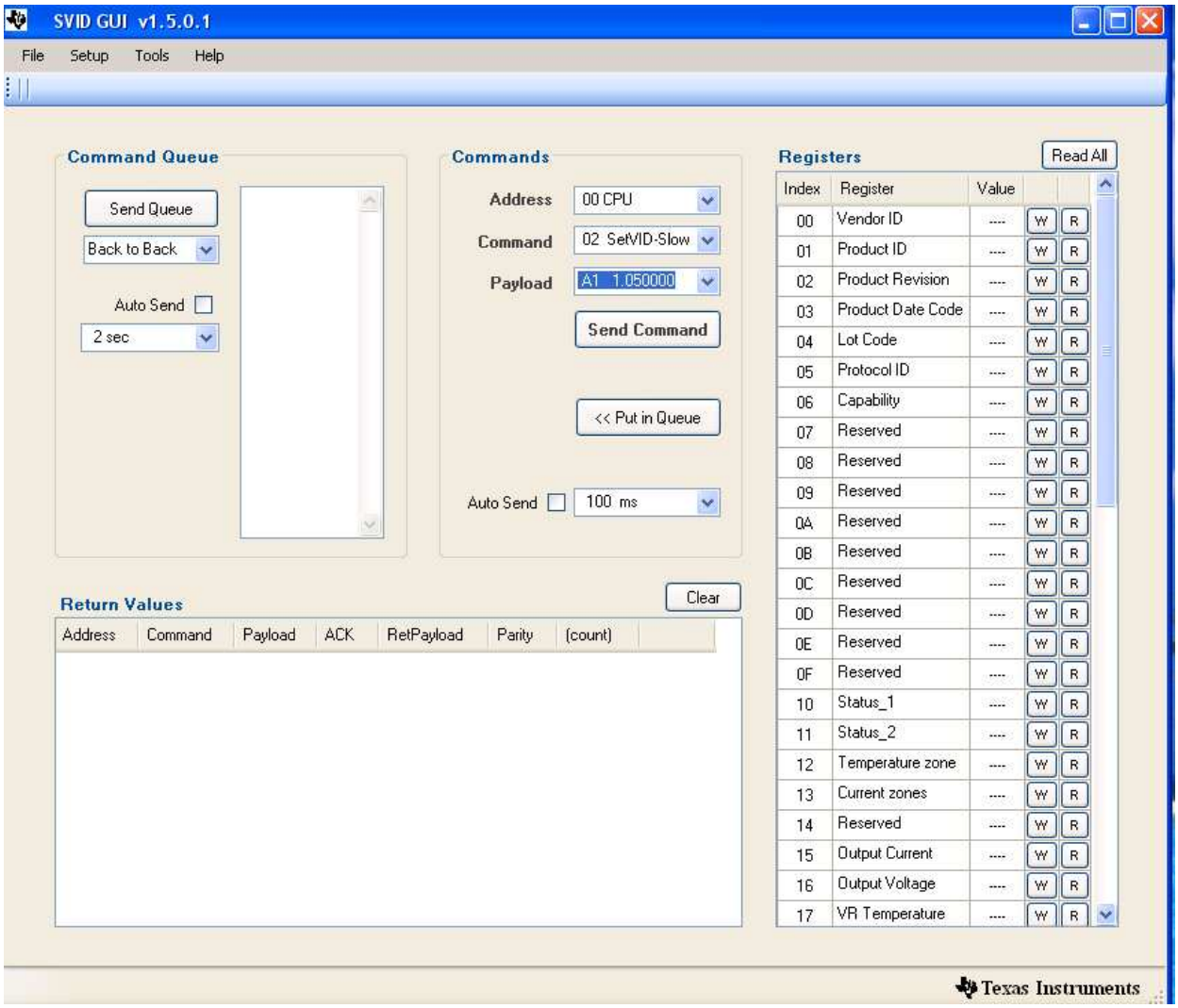


Figure 18. TPS59640EVM-751 CPU GUI Setup Window

7.1.2 GPU

1. Connect the LOAD to GPU terminal J11 and V3 at J16. Ensure correct polarity.
2. Add scope probe on the TP37 for GPU G_Vcore ripple measurement.
3. Push S4 to *ON* position to enable the VR_ON of TPS59640. The VR_ON LED lights up.
4. Now you are ready to send SVID commends for GPU. Using the pulldown menu:
   Address: 01 GPU, Commend: SetVIDslow, Payload: 1.23V
5. Click *send Commend*, and GPU GPOOD LED lights up. See the GUI window shown Figure 19.
6. Measure V3: GPU G_Vcore at J16 and A1: 12VBAT input current.
7. Vary GPU LOAD from 0 Adc to 30 Adc; GPU Vcore must remain in load line.
8. Vary 12VBAT from 9 V to 20 V; GPU Vcore must remain in line regulation.
9. Push S4 to *OFF* position to disable GPU Vcore controller.
10. Decrease LOAD to 0 A, and disconnect the LOAD from terminal J11.
11. Disconnect V3 from J16.
12. Disconnect scope probe from TP37.
13. Exit SVID GUI window: click File → click Exit.

Copyright © 2012, Texas Instruments Incorporated

14. Disconnect the USB cable between host Computer and EVM.

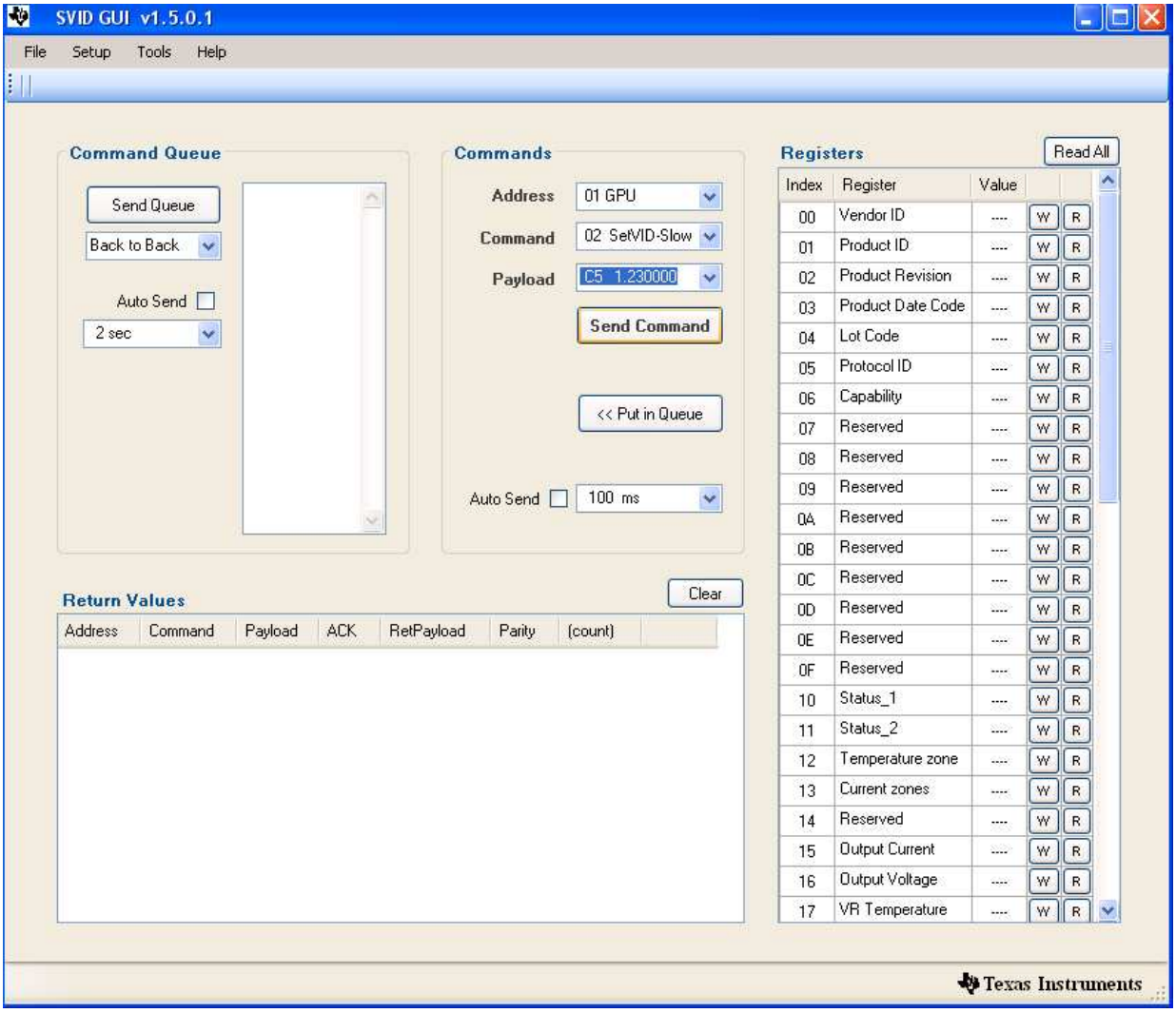


Figure 19. TPS59640EVM-751 GPU GUI Setup Window

7.1.3 VDDQ

1. Connect the LOAD to VDDQ terminal J28 and V3 at J29. Ensure correct polarity.
2. Remove jumper from J27 from pin 2 and pin 3, and put this jumper on pin 1 and pin 2 of J27 to enable S5 of VDDQ controller. VDDQ PGOOD LED lights up.
3. Measure V3: VDDQ at J29 and A1: 12Vin input current
4. Vary VDDQ LOAD from 0 Adc to 15 Adc; VDDQ must remain in the load regulation.
5. Vary 12VBAT from 9 V to 20 V; VDDQ must remain in the line regulation.
6. Remove jumper off J27, and short back on pin 2 and pin 3 of J27 to disable VDDQ controller.
7. Decrease LOAD to 0 A, and disconnect the LOAD from terminal J28.
8. Disconnect V3 from J29.

7.1.4 VCCIO

1. Connect the LOAD to VCCIO terminal J24 and V3 at J25. Ensure correct polarity.
2. Push S1 to *ON* position to enable the VCCIO controller. VCCIO EN and PGOOD LEDs light up.

Copyright © 2012, Texas Instruments Incorporated

3. Measure V3: VCCIO at J25 and A1: 12Vin input current.
4. Vary VDDQ LOAD from 0 Adc to 15 Adc; VCCIO must remain in the load regulation.
5. Vary 12VBAT from 9 V to 20 V; VCCIO must remain in the line regulation.
6. Push S1 to *OFF* position to disable VCCIO controller.
7. Decrease LOAD to 0 A, and disconnect the LOAD from terminal J24.
8. Disconnect V3 from J25.

7.2 Equipment Shutdown

1. Shut down load.
2. Shut down 12VBAT and 5Vin.
3. Shut down oscilloscope.
4. Shut down host computer.

Copyright © 2012, Texas Instruments Incorporated

8 Performance Data and Typical Characteristic Curves

Figure 20 through Figure 91 present typical performance curves for TPS59640EVM-751. Jumpers are set to default locations; see Section 6 of this user's guide

8.1 CPU3-Phase Operation

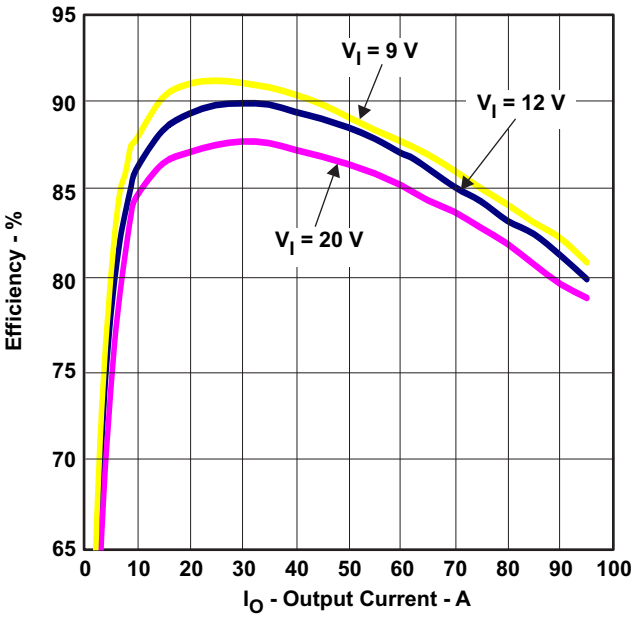


Figure 20. CPU3 Efficiency

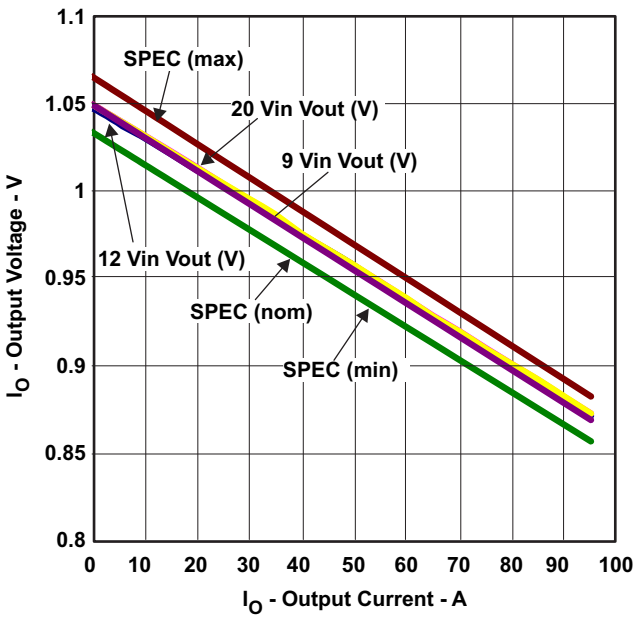


Figure 21. CPU3 Load Regulation

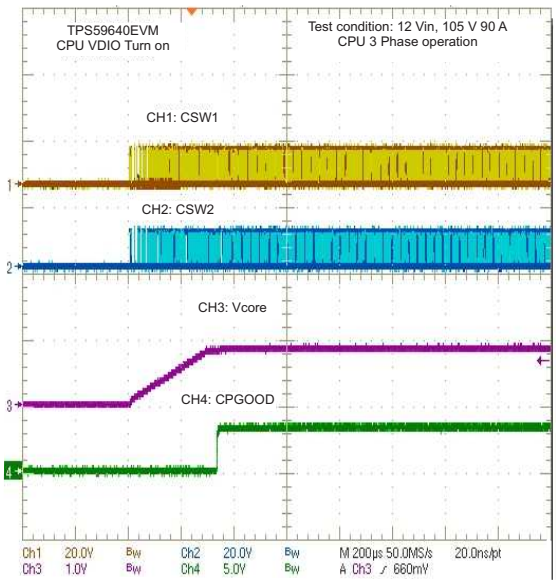


Figure 22. CPU3 Enable Turnon

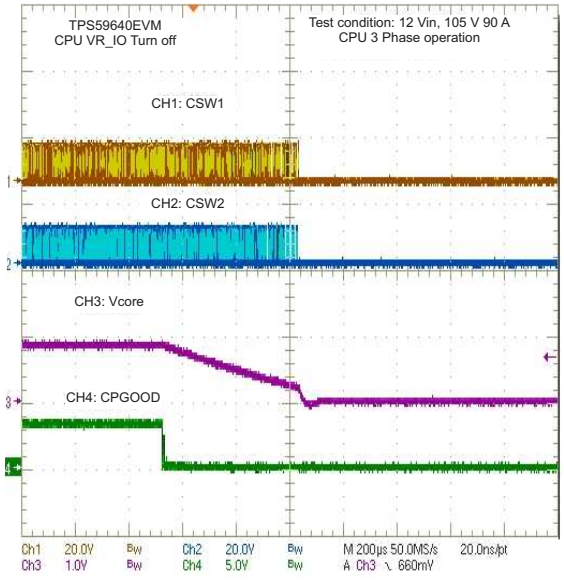


Figure 23. CPU3 Enable Turnoff

Copyright © 2012, Texas Instruments Incorporated

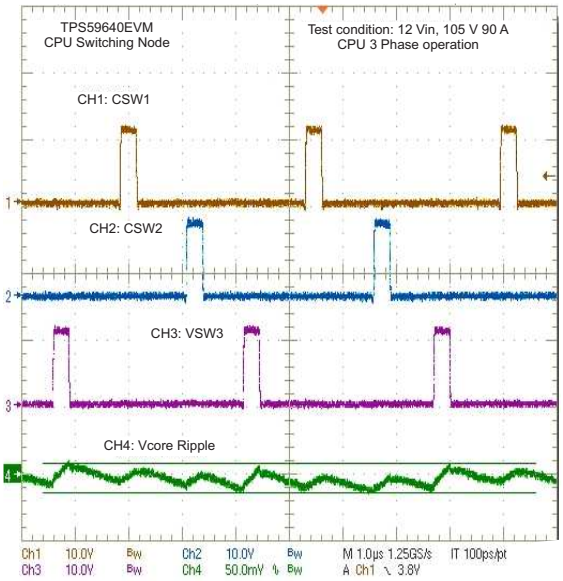


Figure 24. CPU3 Switching Node (Ripple)

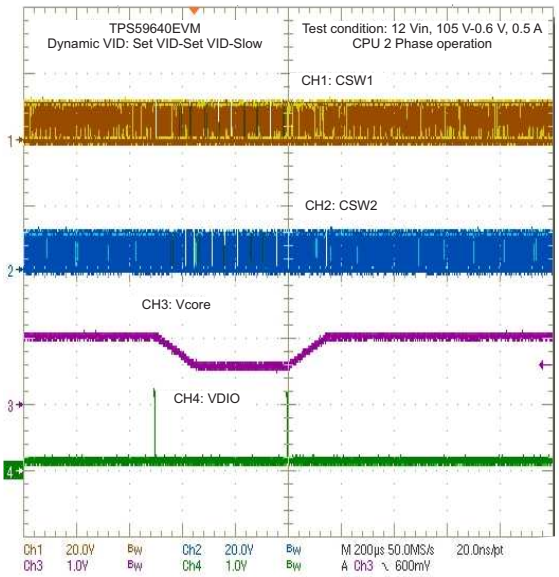


Figure 25. CPU3 Dynamic VID: SetVID-Slow/Slow

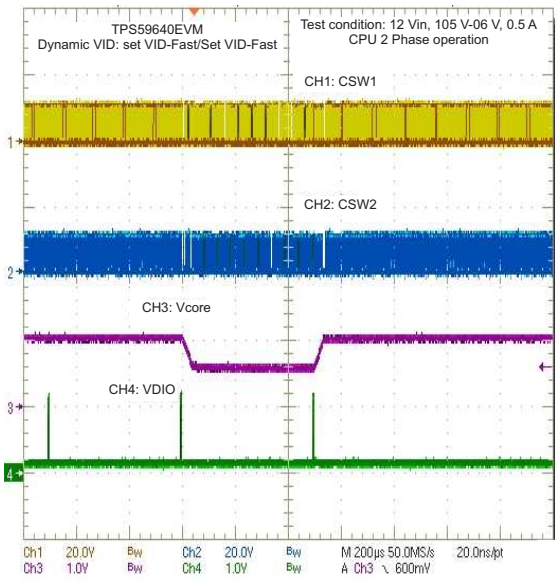


Figure 26. CPU3 Dynamic VID:SetVID-Fast/Fast

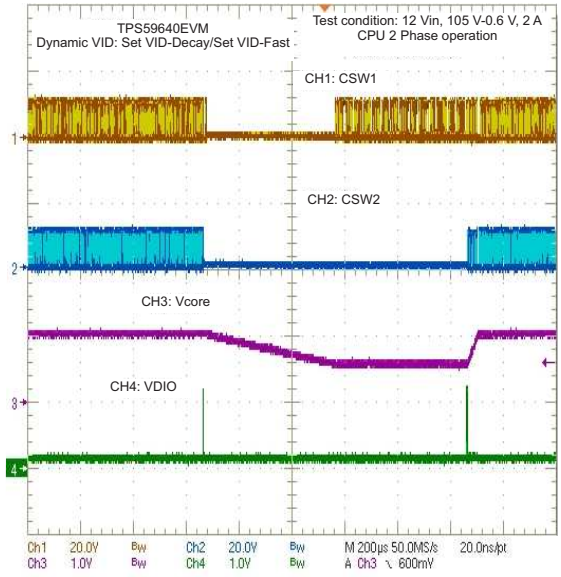


Figure 27. CPU3 Dynamic VID:SetVID-Decay/Fast

Copyright © 2012, Texas Instruments Incorporated

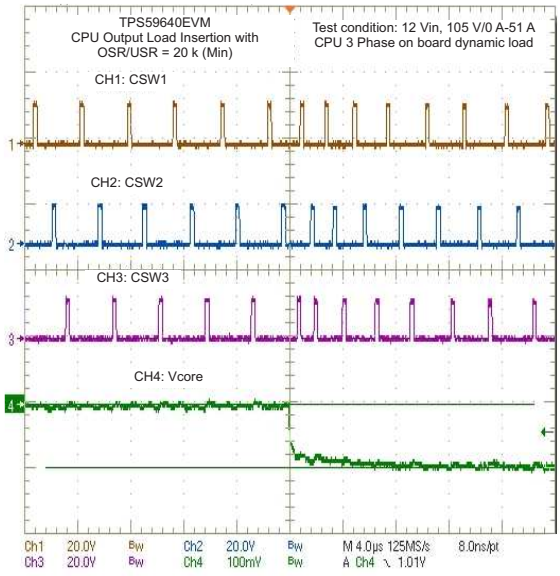


Figure 28. CPU3 Output Load Insertion With OSR/USR20k (Min)

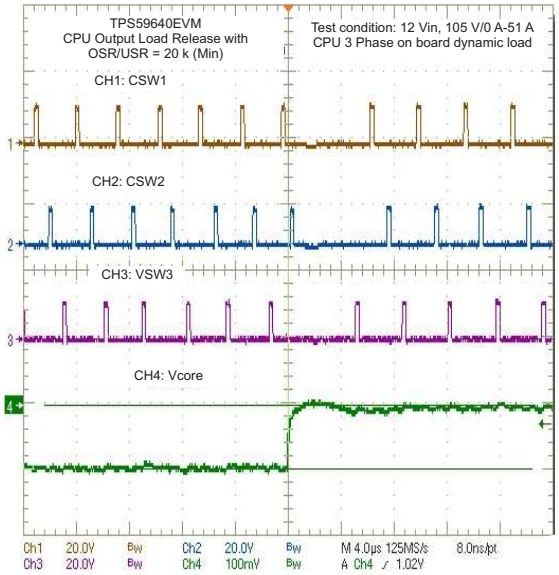


Figure 29. CPU3 Output Load Release With OSR/USR 20k (Min)

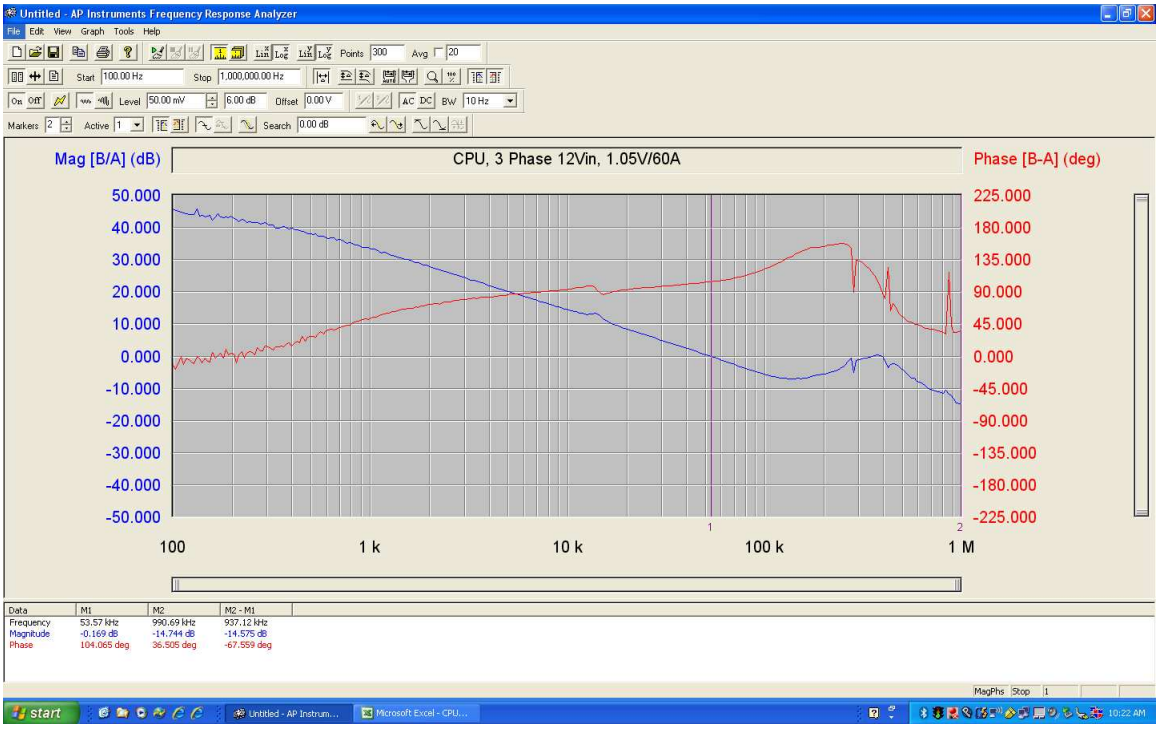


Figure 30. CPU3 Bode Plot at 12Vin, 1.05 V/60 A

Copyright © 2012, Texas Instruments Incorporated

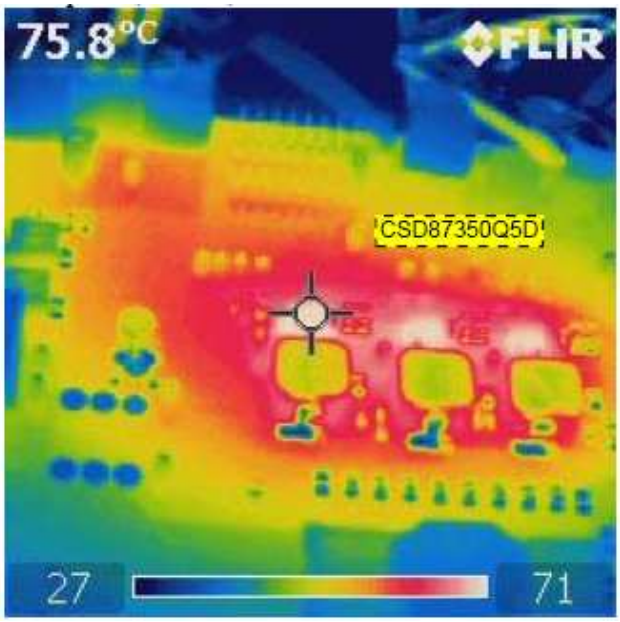


Figure 31. CPU3 MOSFET

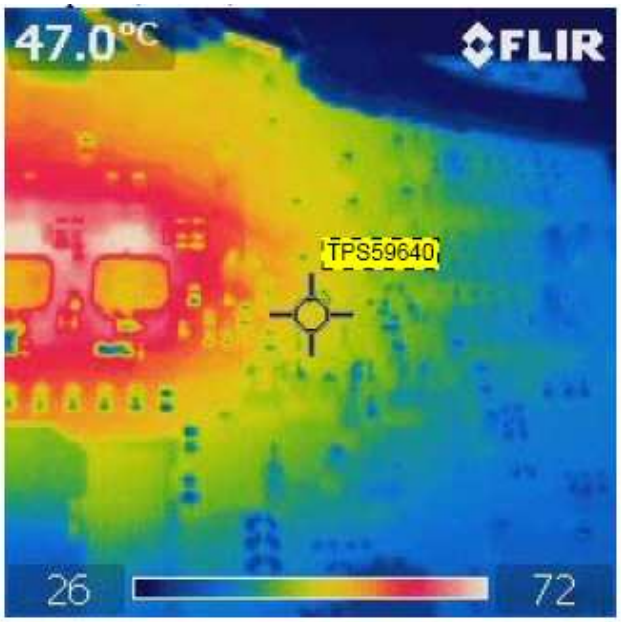


Figure 32. CPU3 IC

Test condition: CPU3 12Vin, 1.05 V/60 A, no airflow

Copyright © 2012, Texas Instruments Incorporated

8.2 CPU 2-Phase Operation

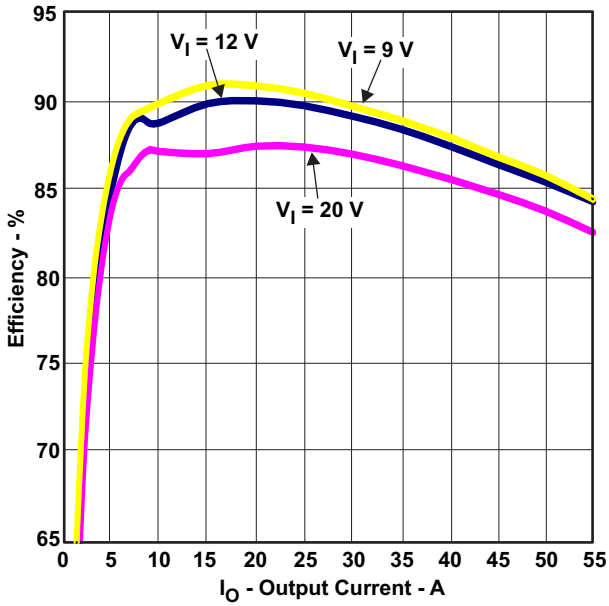


Figure 33. CPU2 Efficiency

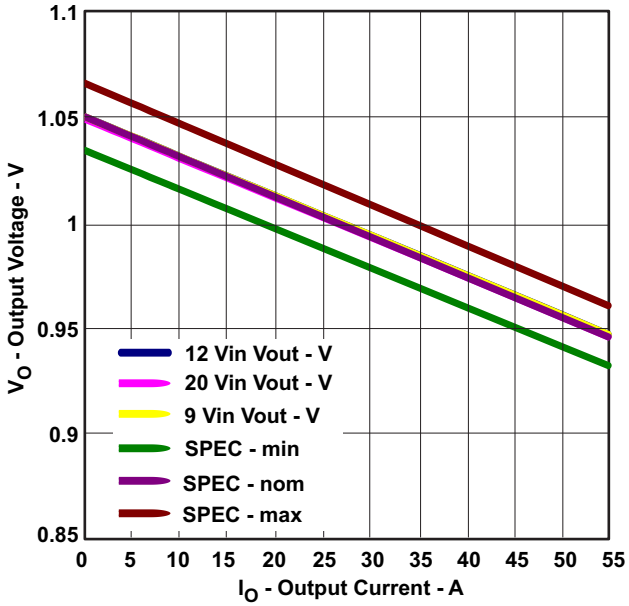


Figure 34. CPU2 Load Regulation

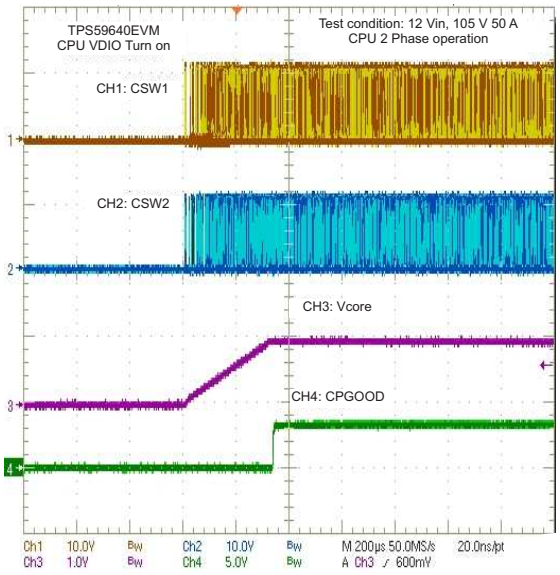


Figure 35. CPU2 Enable Turnon

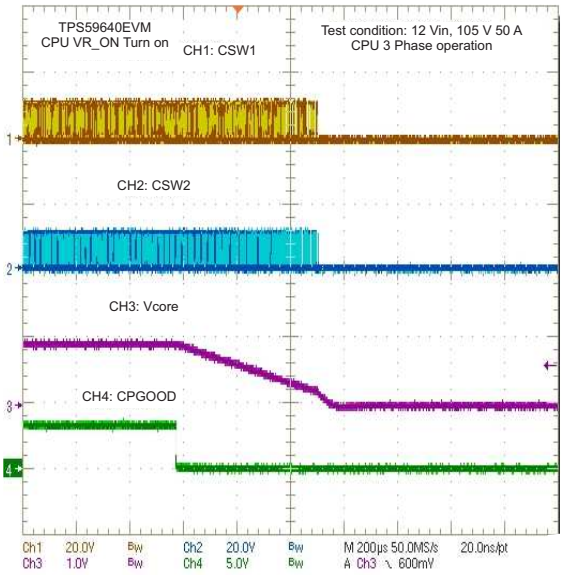


Figure 36. CPU2 Enable Turnoff

Copyright © 2012, Texas Instruments Incorporated

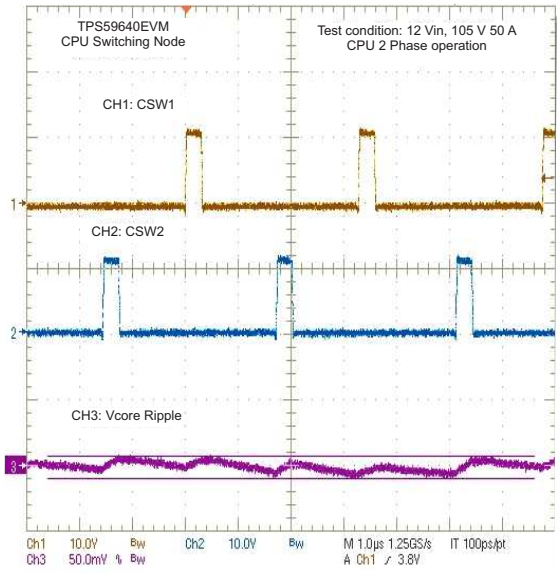


Figure 37. CPU2 Switching Node (Ripple)

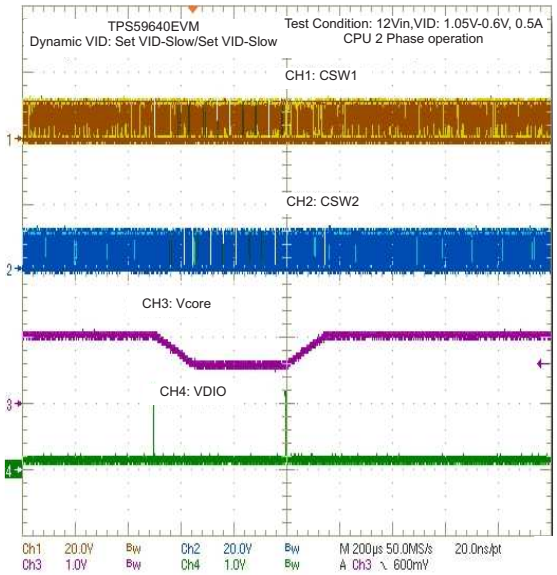


Figure 38. CPU2 Dynamic VID: SetVID-Slow/Slow

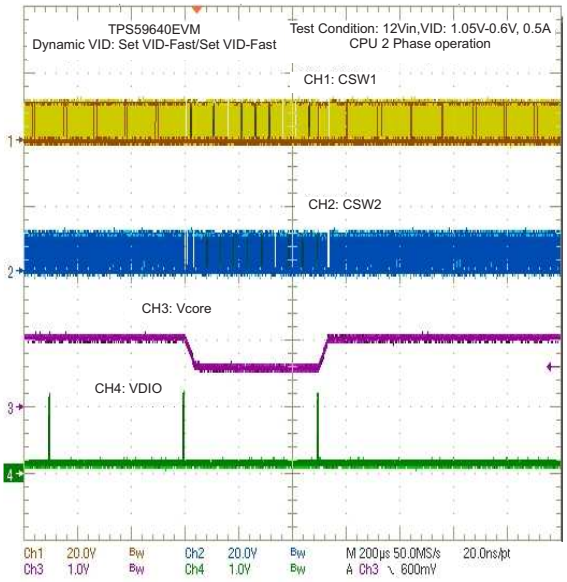


Figure 39. CPU2 Dynamic VID: SetVID-Fast/Fast

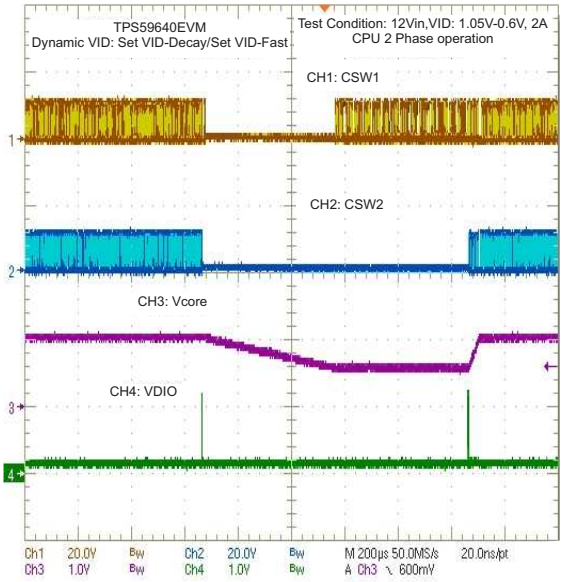


Figure 40. CPU2 Dynamic VID: SetVID-Decay/Fast

Copyright © 2012, Texas Instruments Incorporated

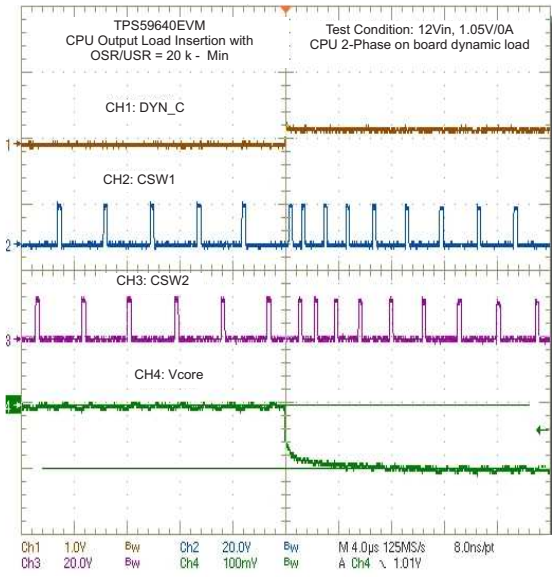


Figure 41. CPU2 Output Load Insertion With OSR/USR 20k (Min)

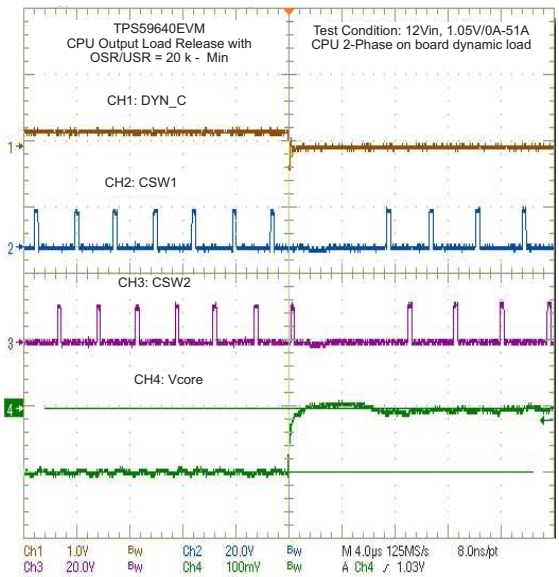


Figure 42. CPU2 Output Load Release With OSR/USR 20k (Min)

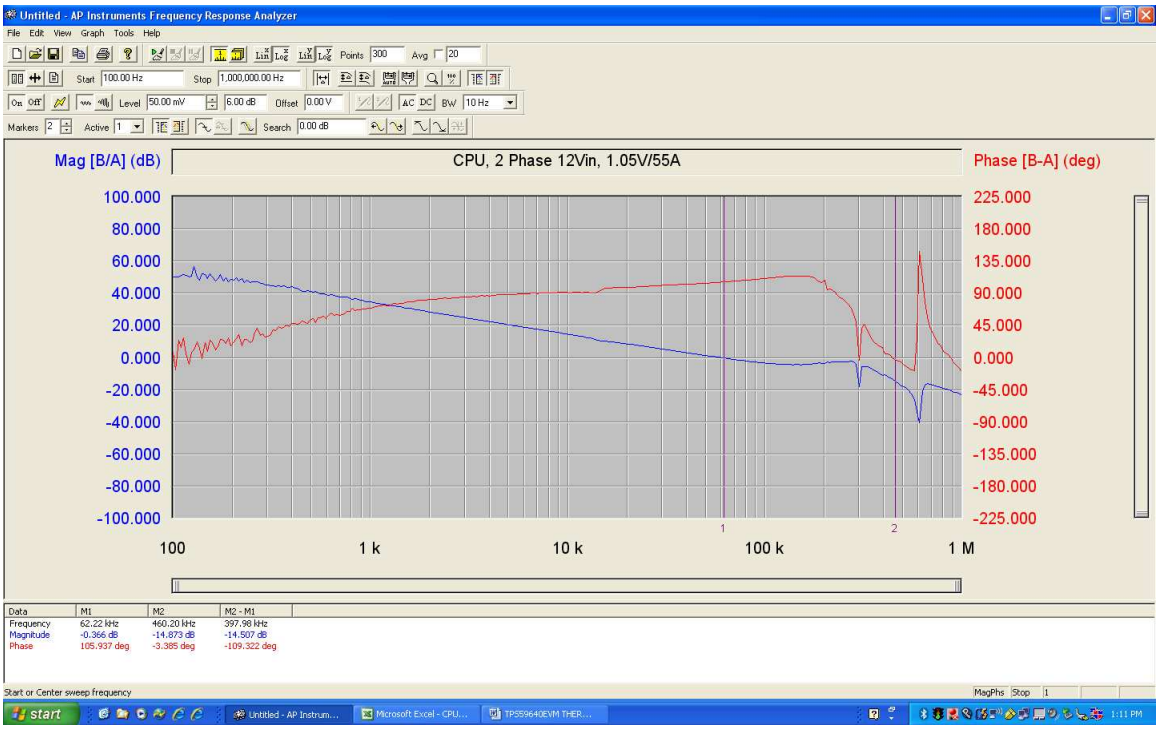


Figure 43. CPU2 Bode Plot at 12Vin, 1.05 V/55 A

Copyright © 2012, Texas Instruments Incorporated

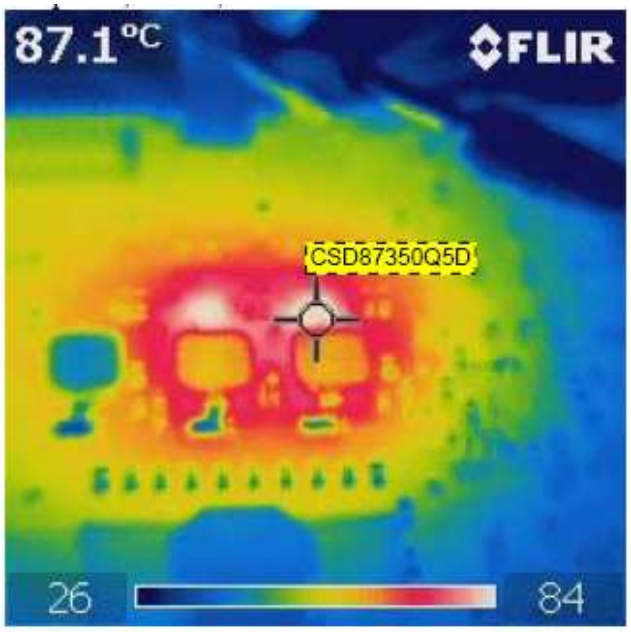


Figure 44. CPU2 MOSFET

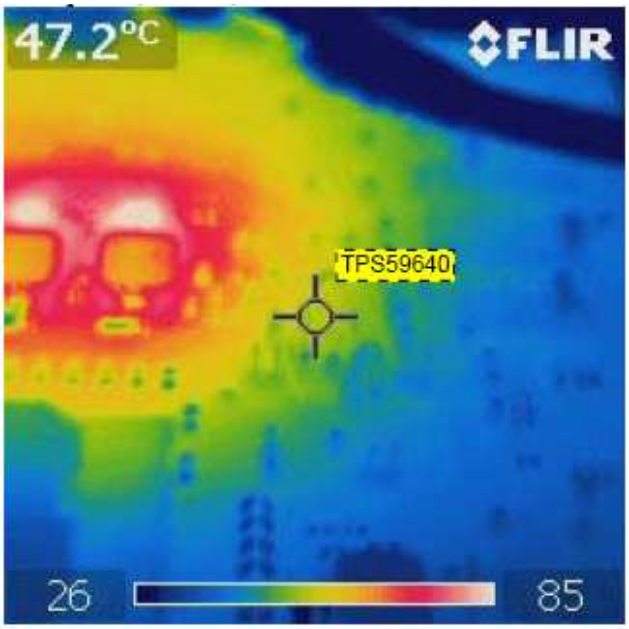


Figure 45. CPU2 IC

Test condition: CPU2 12Vin, 1.05 V/55 A, no airflow

Copyright © 2012, Texas Instruments Incorporated

8.3 CPU 1-Phase Operation

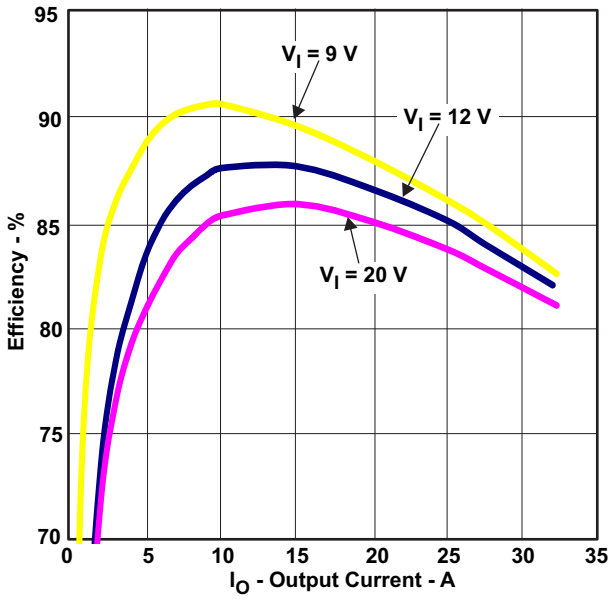


Figure 46. CPU1 Efficiency

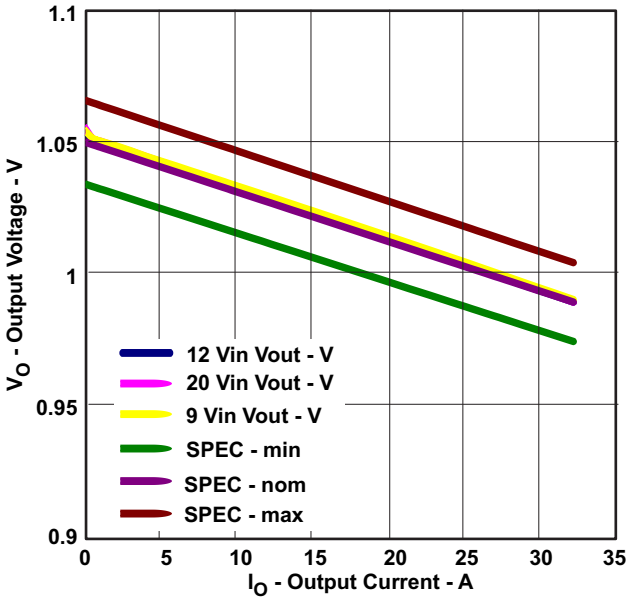


Figure 47. CPU1 Load Regulation

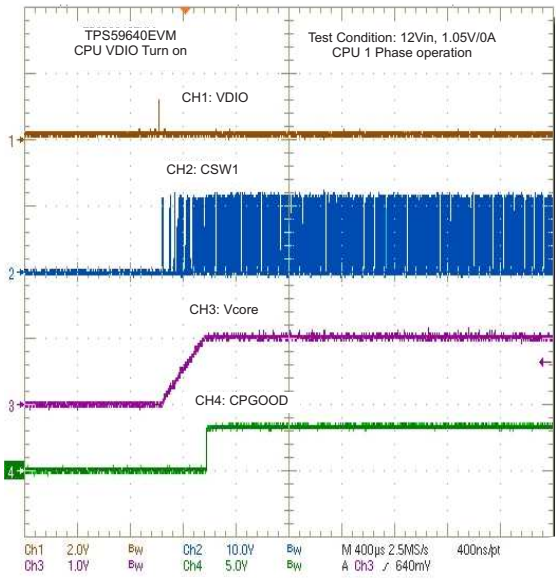


Figure 48. CPU1 Enable Turnon

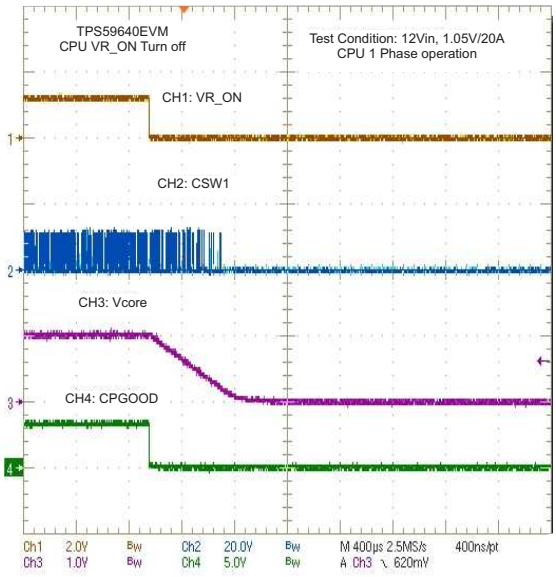


Figure 49. CPU1 Enable Turnoff

Copyright © 2012, Texas Instruments Incorporated

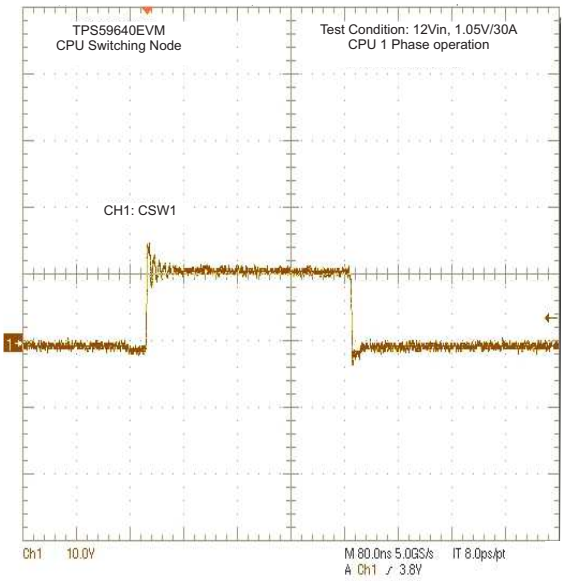


Figure 50. CPU1 Switching Node

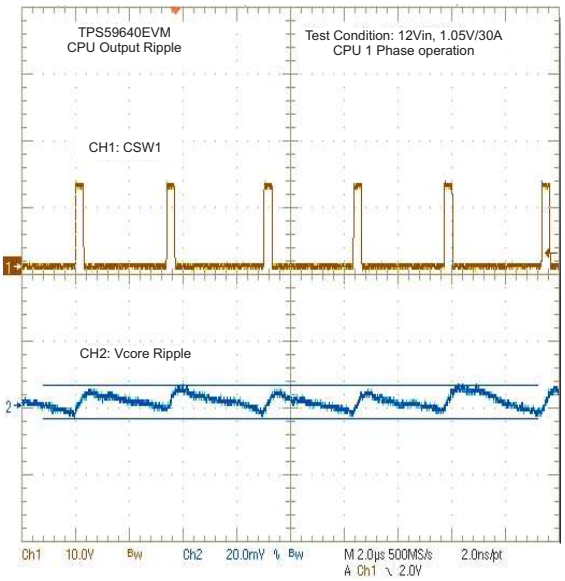


Figure 51. CPU1 Switching Node and Ripple

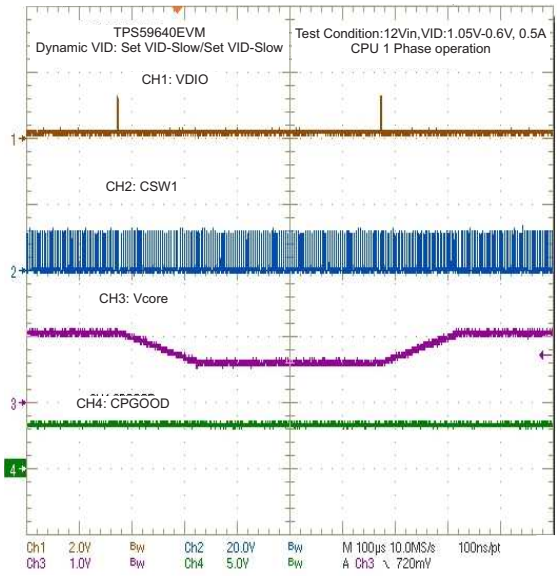


Figure 52. CPU1 Dynamic VID: SetVID-Slow/Slow

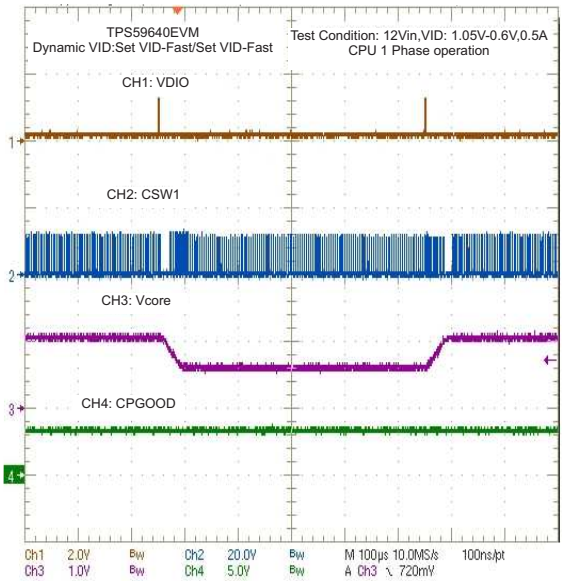


Figure 53. CPU1 Dynamic VID: SetVID-Fast/Fast

Copyright © 2012, Texas Instruments Incorporated

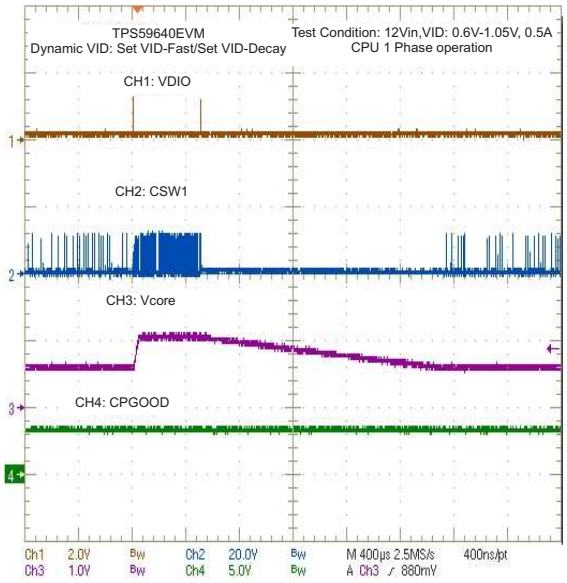


Figure 54. CPU1 Dynamic VID: SetVID-Decay/Fast

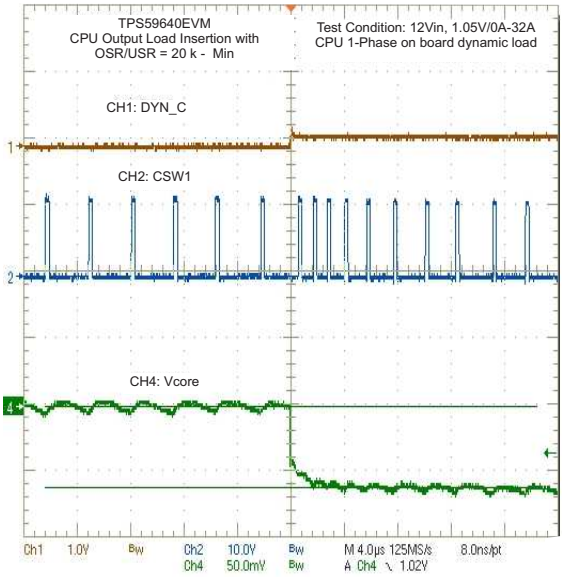


Figure 55. CPU1 Output Load Insertion With OSR/USR 20k (Min)

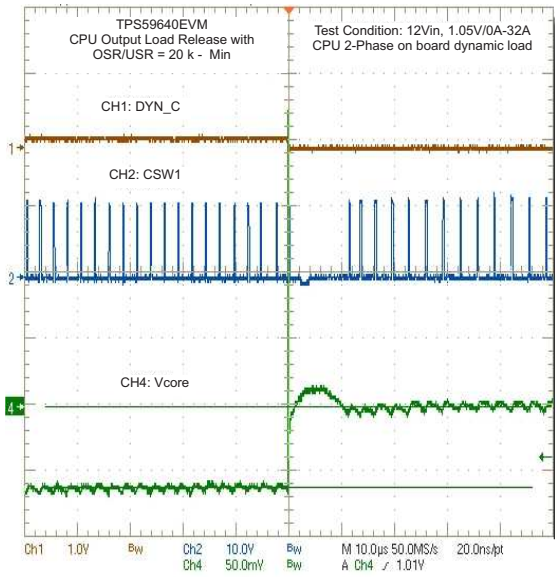


Figure 56. CPU1 Output Load Release With OSR/USR 20k (Min)

Copyright © 2012, Texas Instruments Incorporated

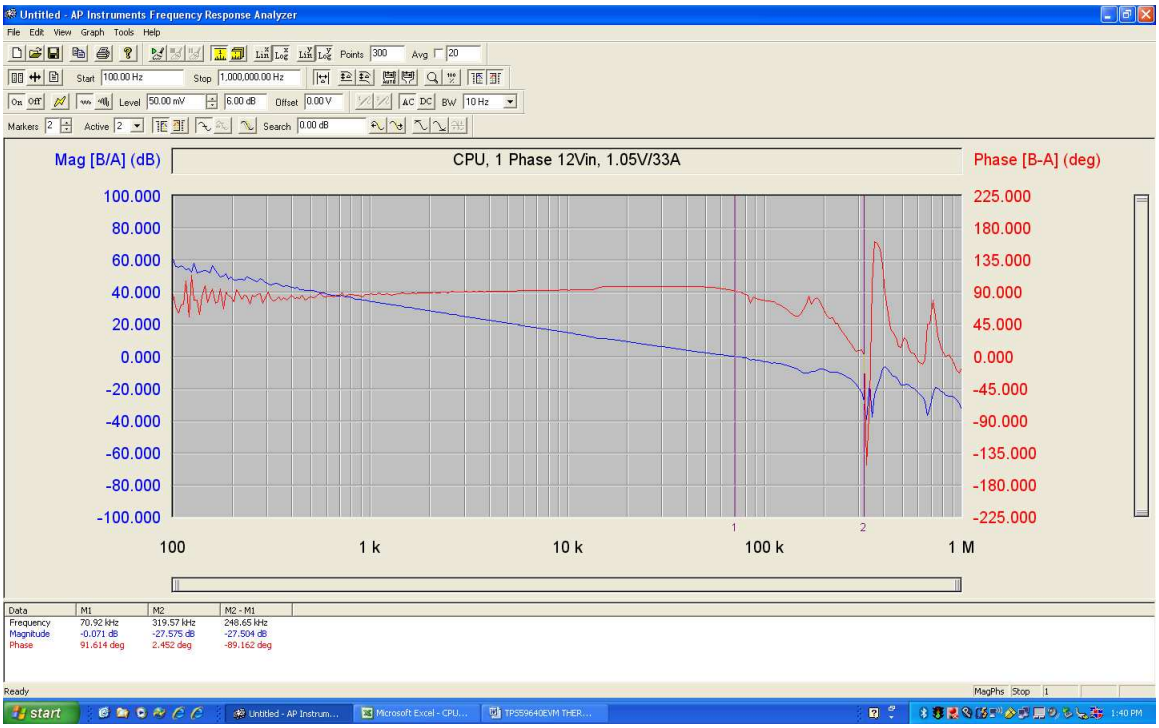


Figure 57. CPU1 Bode Plot at 12Vin, 1.05 V/33 A

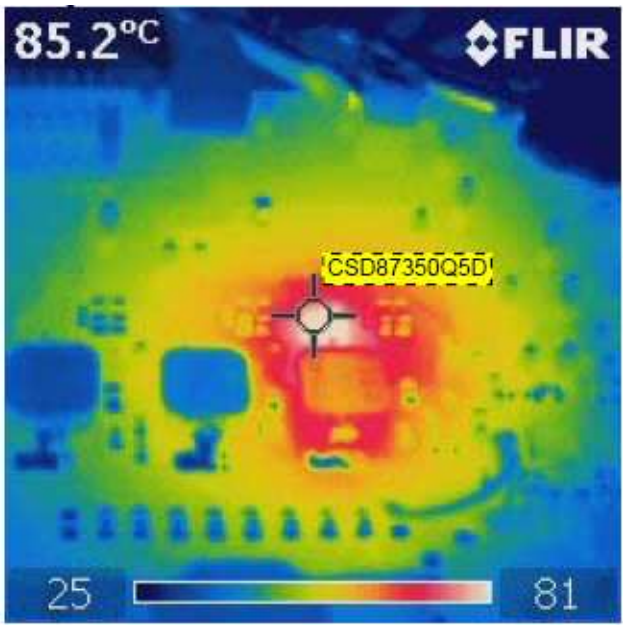


Figure 58. CPU1 MOSFET

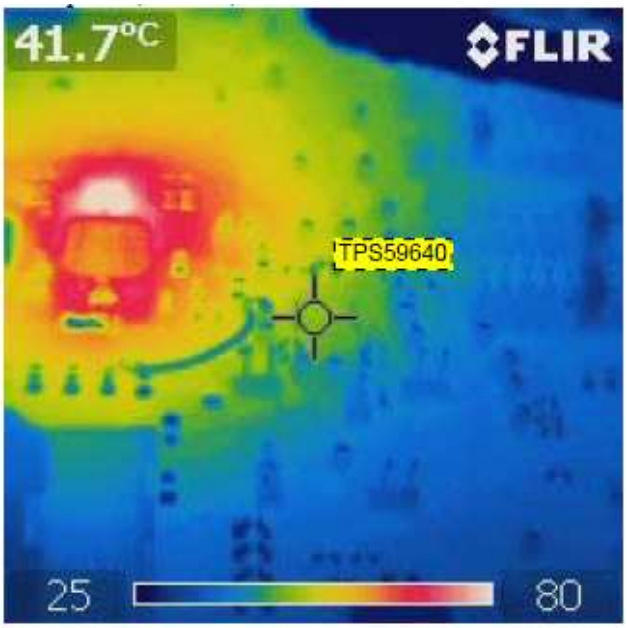


Figure 59. CPU1 IC

Test condition: CPU1 12Vin, 1.05 V/33 A, no airflow

Copyright © 2012, Texas Instruments Incorporated

8.4 GPU Operation

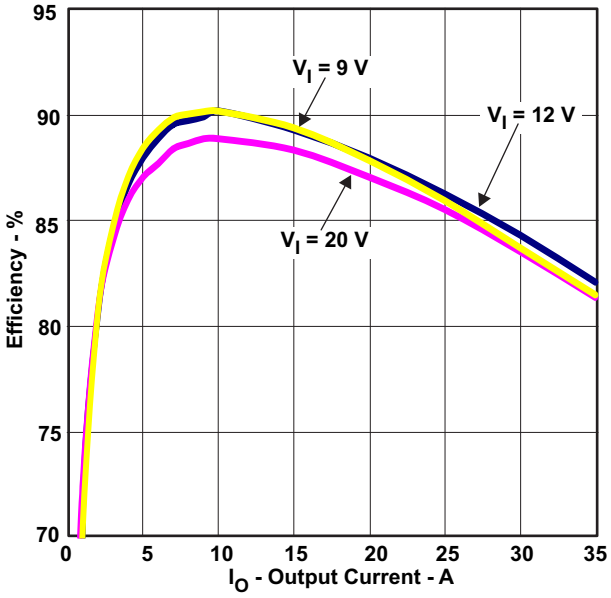


Figure 60. GPU Efficiency

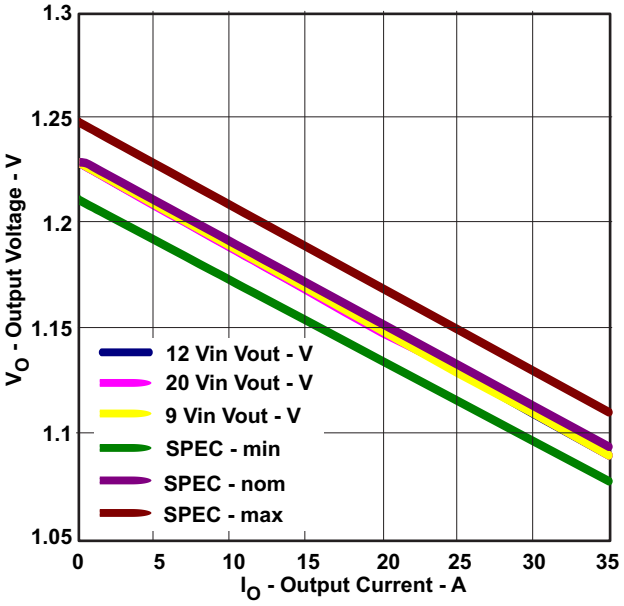


Figure 61. GPU Load Regulation

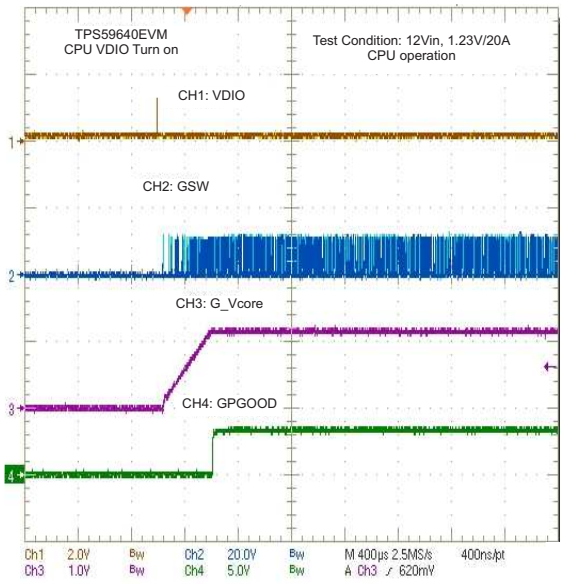


Figure 62. GPU Enable Turnon

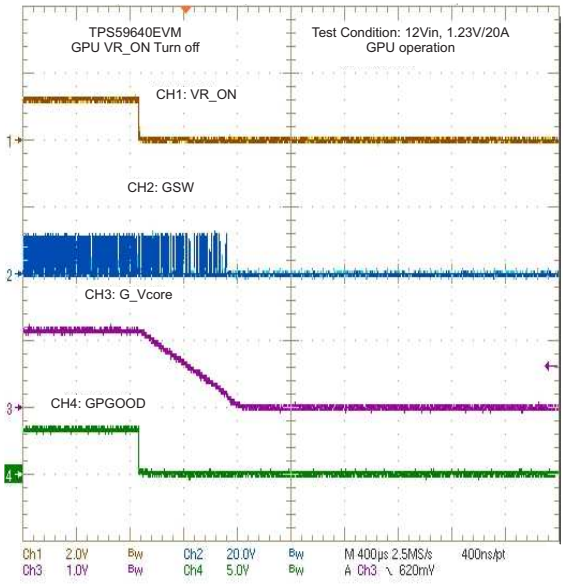


Figure 63. GPU Enable Turnoff

Copyright © 2012, Texas Instruments Incorporated

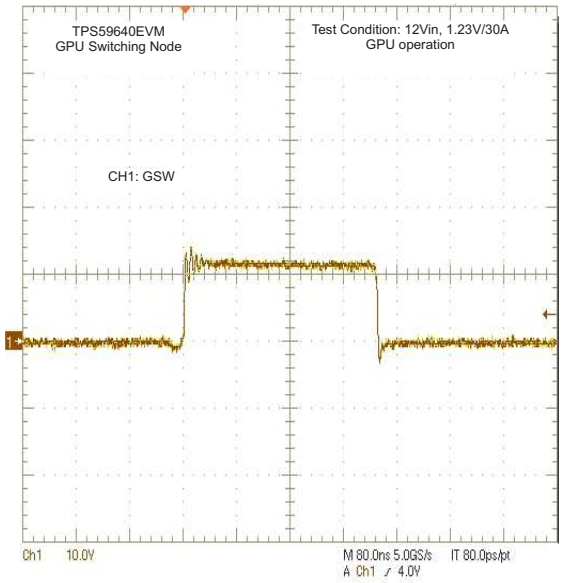


Figure 64. GPU Switching Node

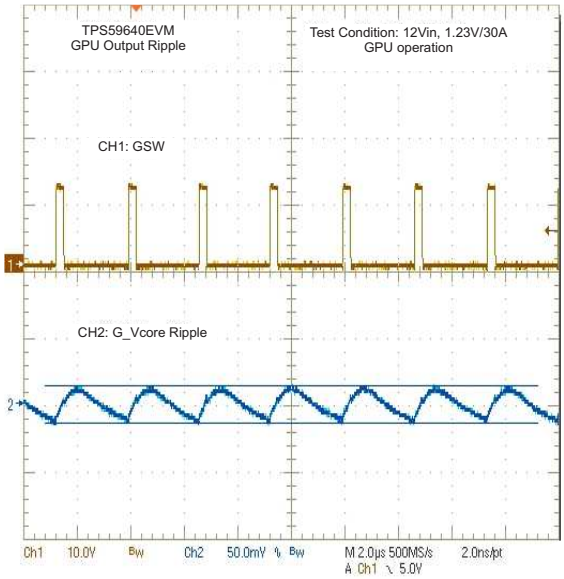


Figure 65. GPU Switching Node and Ripple

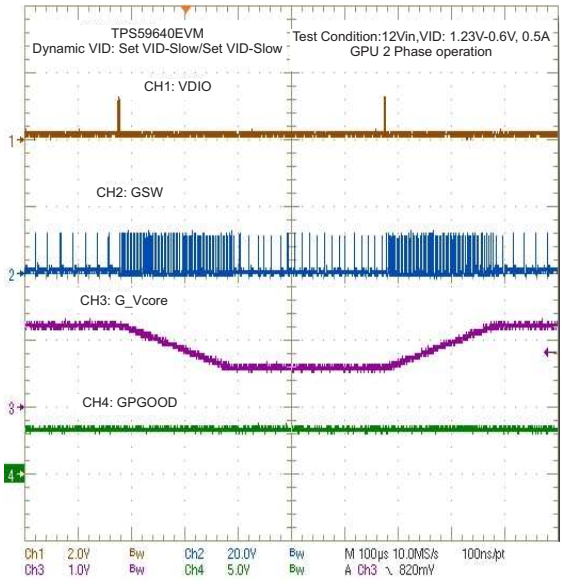


Figure 66. GPU Dynamic VID: SetVID-Slow/Slow

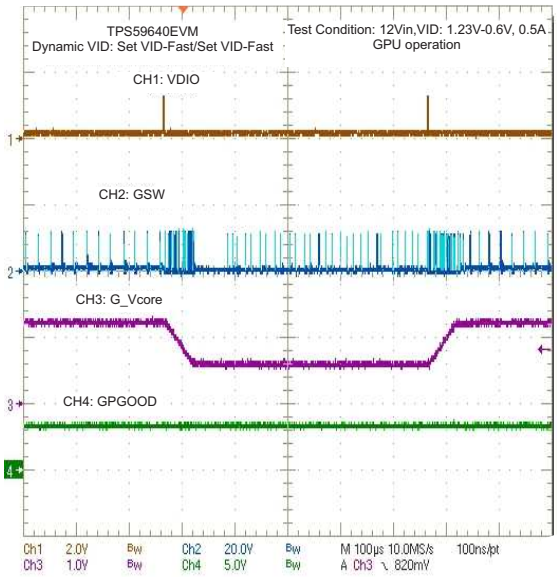


Figure 67. GPU Dynamic VID: SetVID-Fast/Fast

Copyright © 2012, Texas Instruments Incorporated

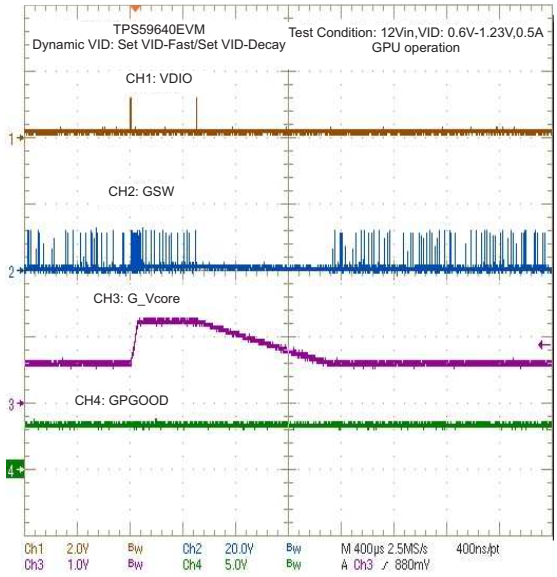


Figure 68. GPU Dynamic VID: SetVID-Decay/Fast

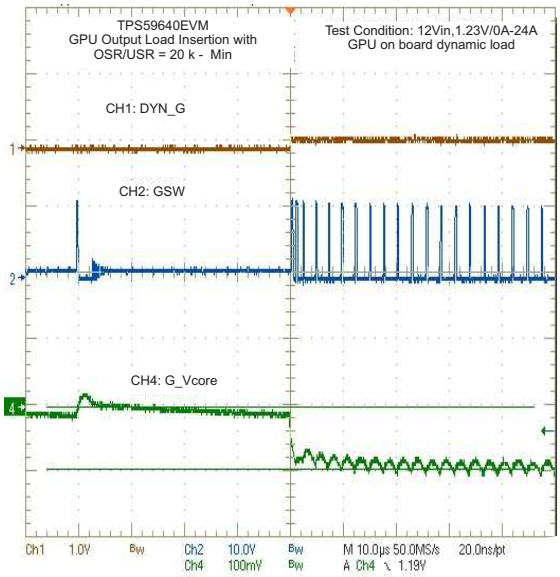


Figure 69. GPU Output Load Insertion With OSR/USR 20k (Min)

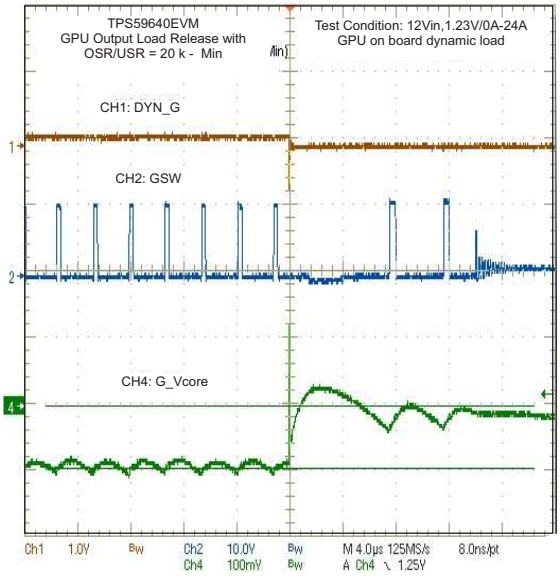


Figure 70. GPU Output Load Release With OSR/USR 20k (Min)

Copyright © 2012, Texas Instruments Incorporated

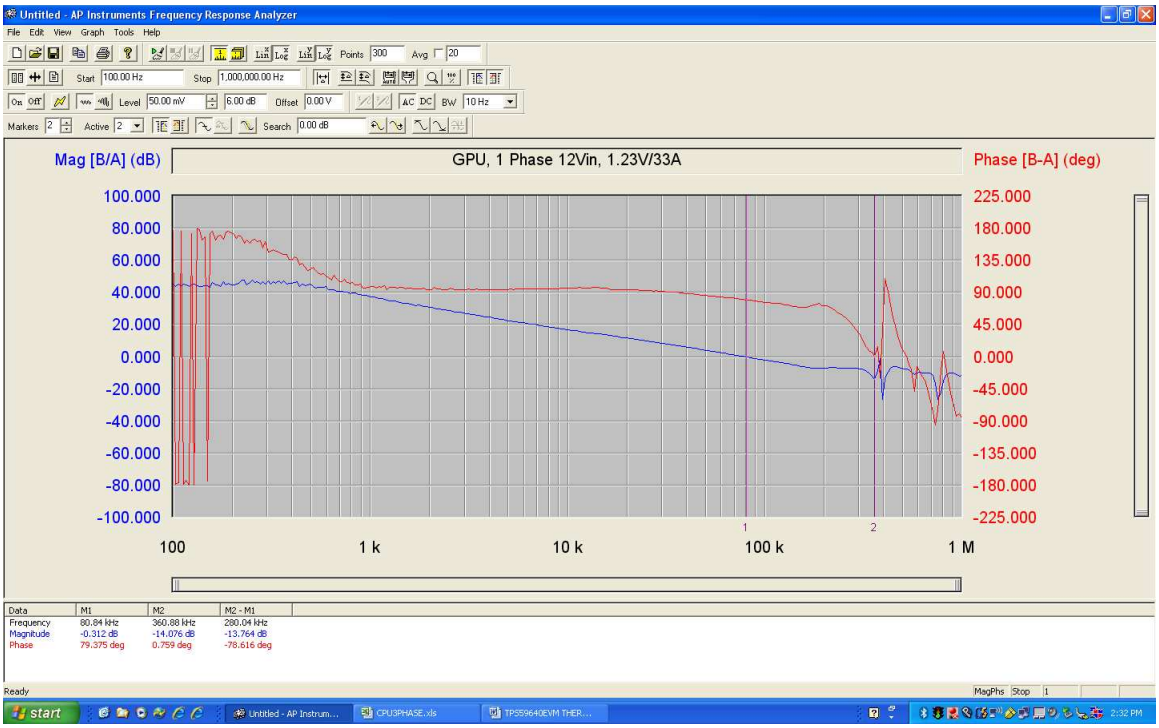


Figure 71. GPU Bode Plot at 12Vin, 1.23 V/33 A

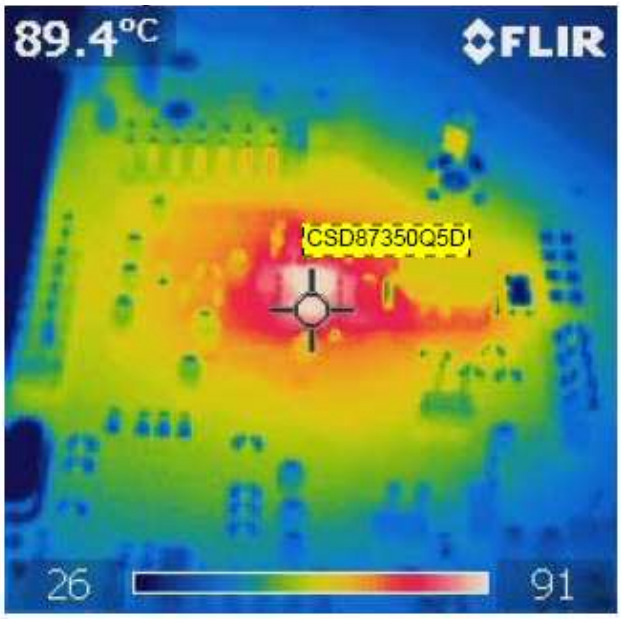


Figure 72. GPU MOSFET

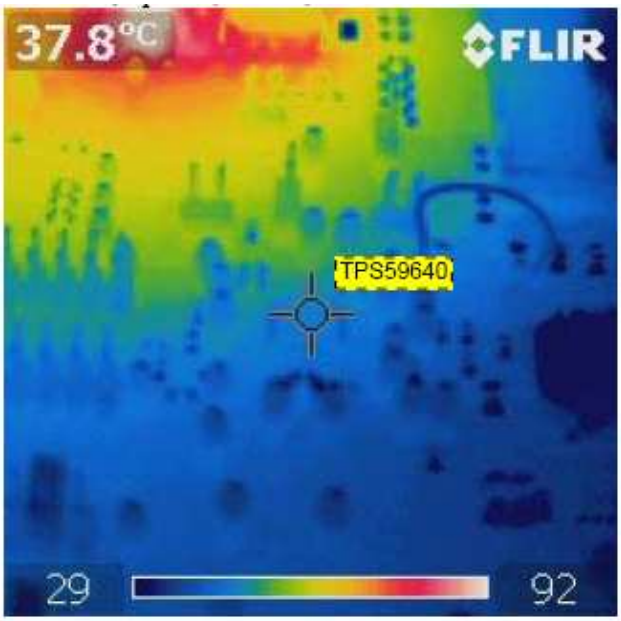


Figure 73. GPU IC

Test condition: GPU 12Vin, 1.23 V/33 A, no airflow

Copyright © 2012, Texas Instruments Incorporated

8.5 1.05V VCCIO

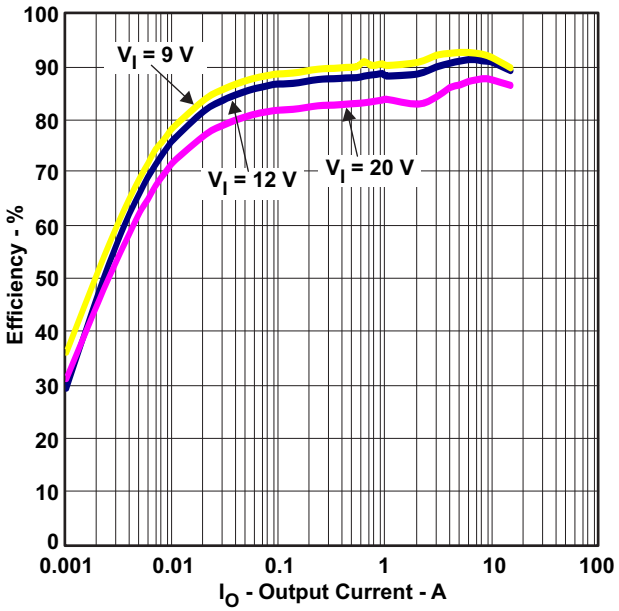


Figure 74. 1.05-V Efficiency

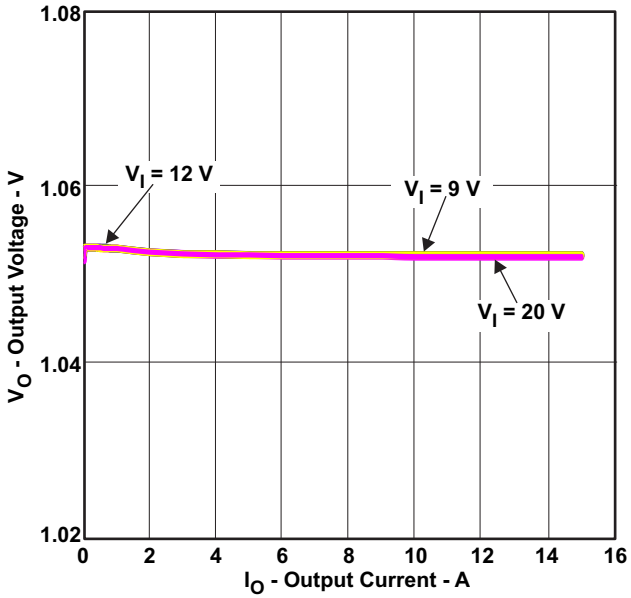


Figure 75. 1.05-V Load Regulation

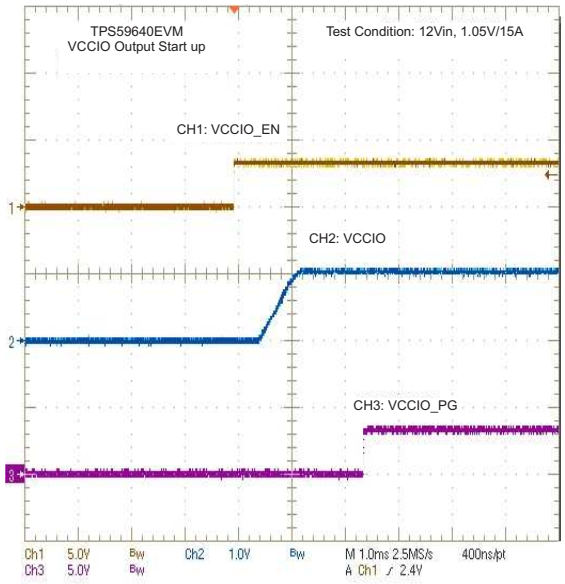


Figure 76. 1.05-V Enable Turnon

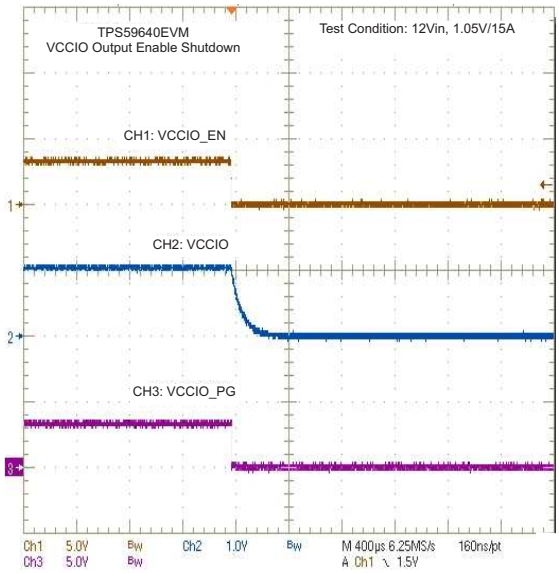


Figure 77. 1.05-V Enable Turnoff

Copyright © 2012, Texas Instruments Incorporated

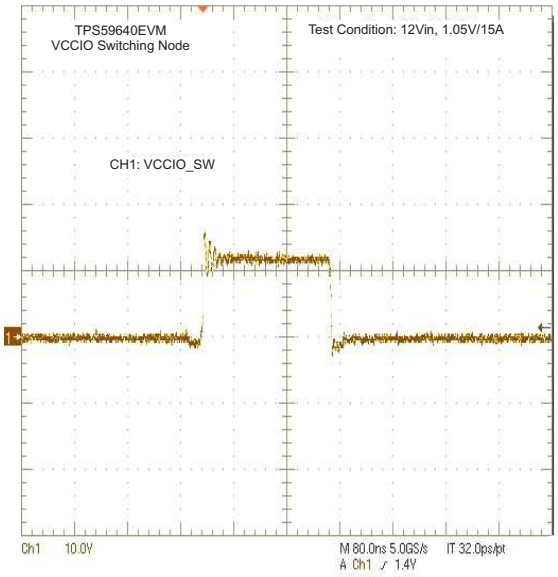


Figure 78. 1.05-V Switching Node

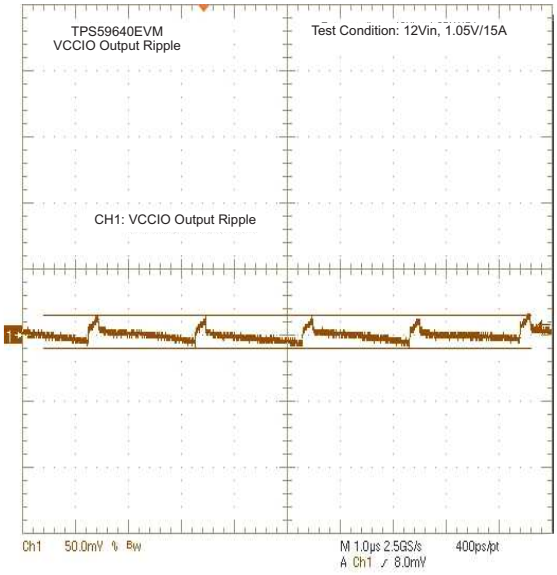


Figure 79. 1.05-V Ripple

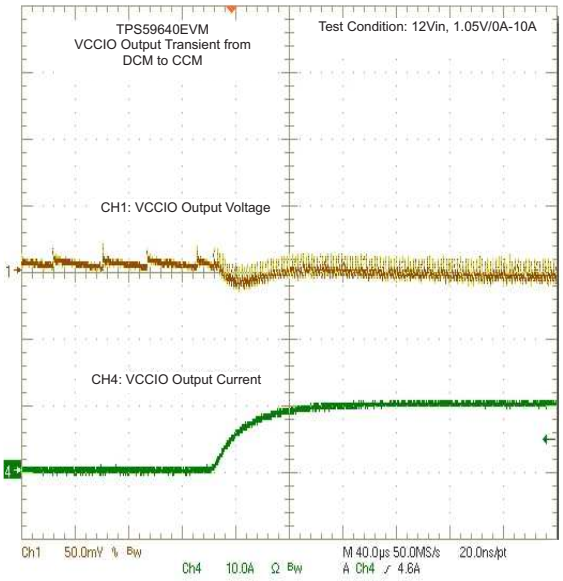


Figure 80. 1.05-V Transient DCM to CCM

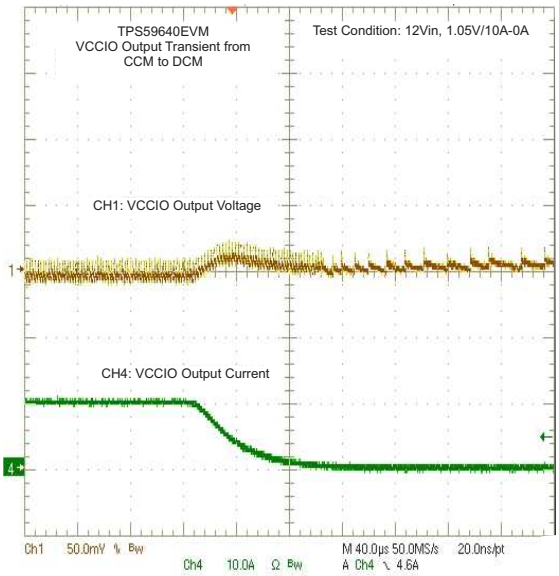


Figure 81. 1.05-V Transient CCM to DCM

Copyright © 2012, Texas Instruments Incorporated

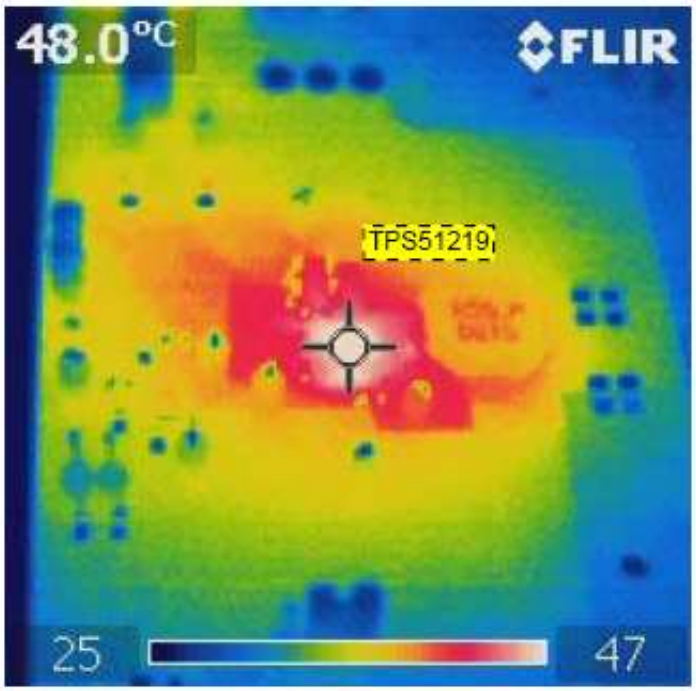


Figure 82. TPS51219 Thermal

Test condition: 12Vin, 1.05 V/15 A, no airflow

Copyright © 2012, Texas Instruments Incorporated

8.6 1.2 VDDQ

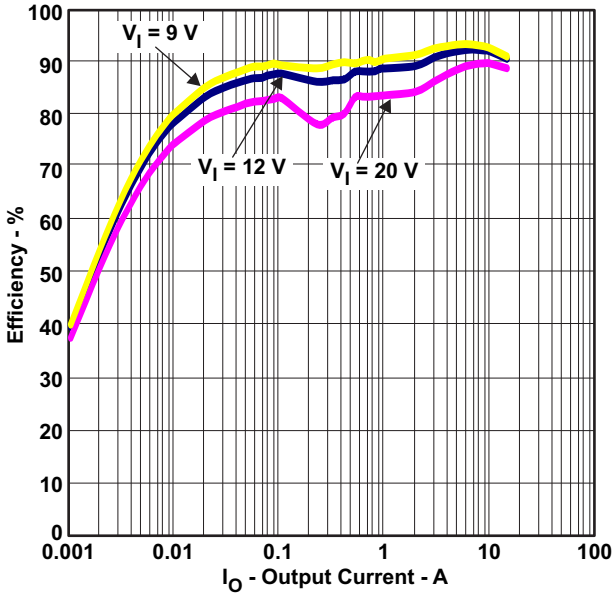


Figure 83. 1.2-V Efficiency

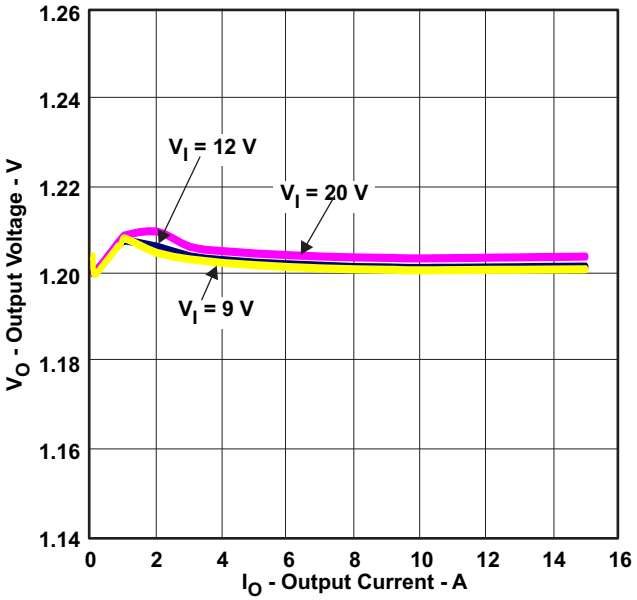


Figure 84. 1.2-V Load Regulation

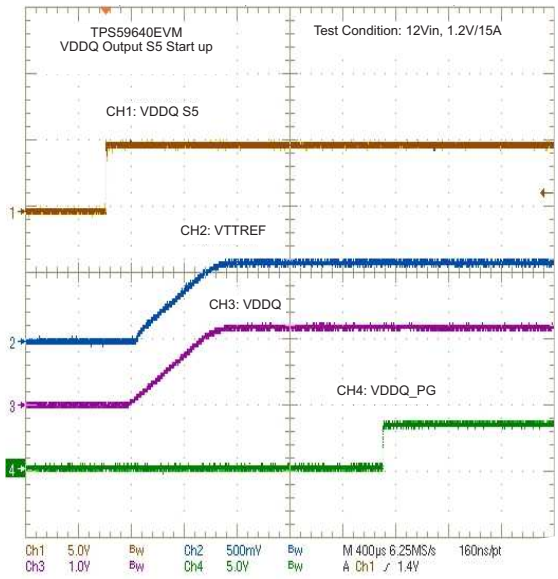


Figure 85. 1.2-V Enable Turnon

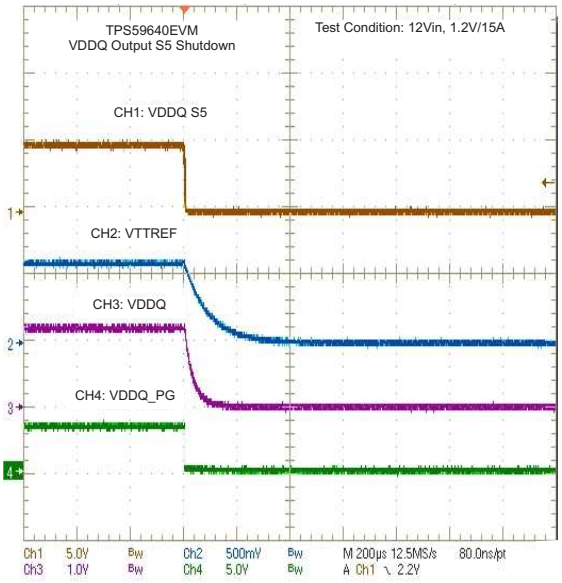


Figure 86. 1.2-V Enable Turnoff

Copyright © 2012, Texas Instruments Incorporated

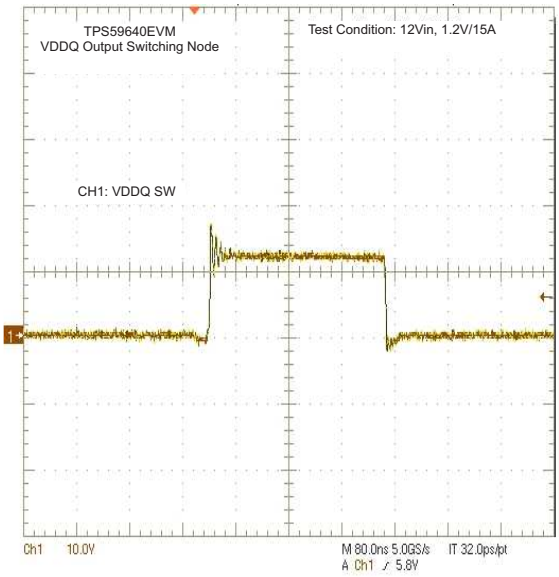


Figure 87. 1.2-V Switching Node

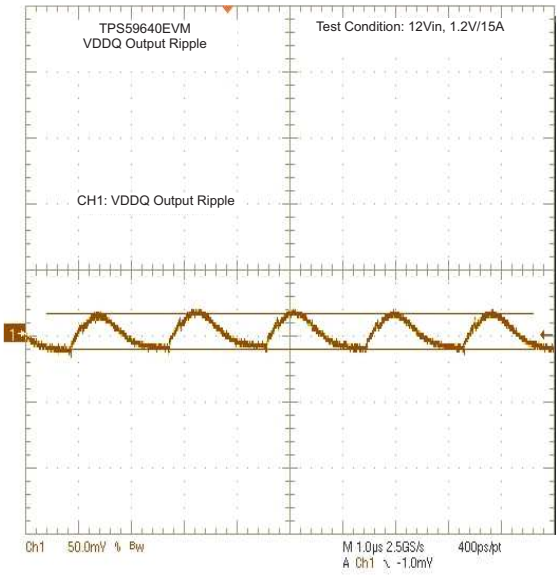


Figure 88. 1.2-V Ripple

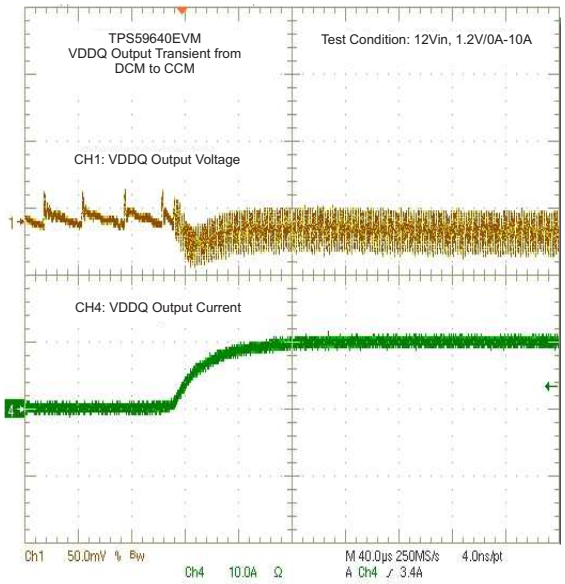


Figure 89. 1.2-V Transient DCM to CCM

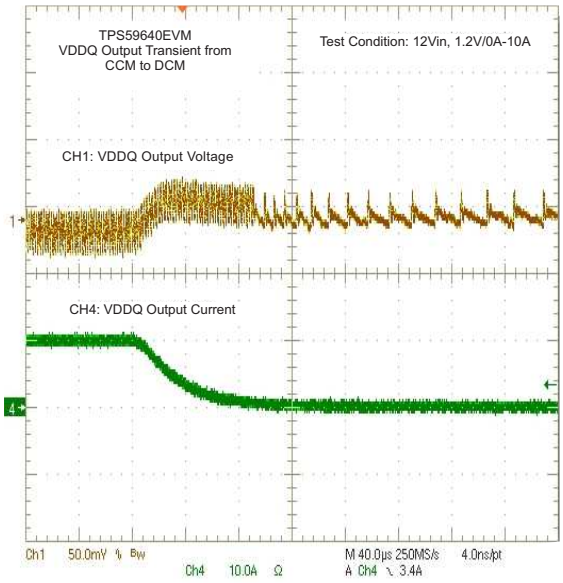


Figure 90. 1.2-V Transient CCM to DCM

Copyright © 2012, Texas Instruments Incorporated

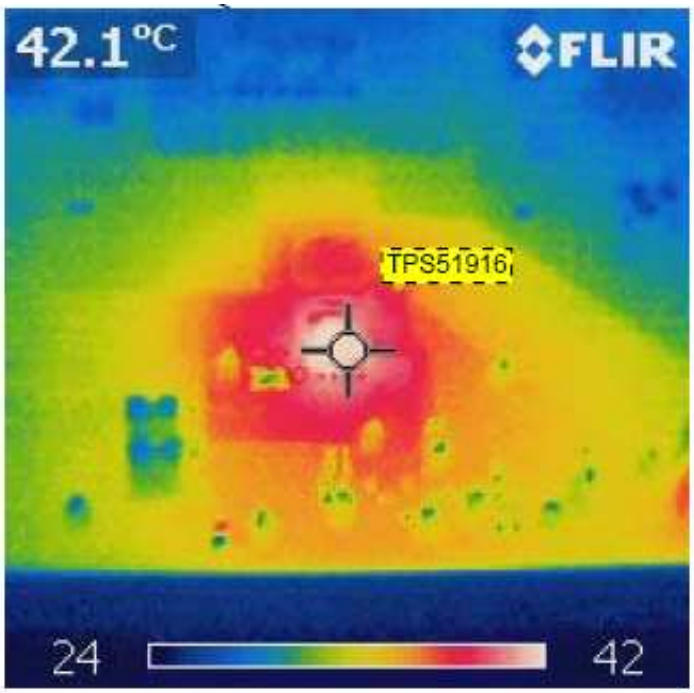


Figure 91. TPS51916 Thermal

Test condition: 12Vin, 1.2 V/15 A, no airflow

9 EVM Assembly Drawings and PCB layout

The following figures (Figure 92 through Figure 101) show the design of the TPS59640EVM-751 printed-circuit board. The EVM has been designed using an eight-layer circuit board with 2 oz o0f copper on outside layers.

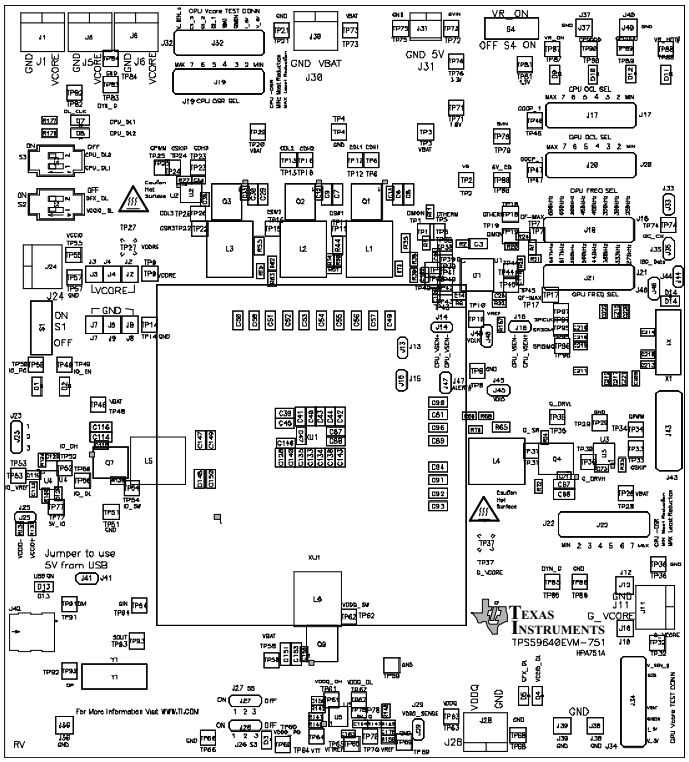


Figure 92. TPS59640EVM-751 Top Layer Assembly Drawing (Top View)

Copyright © 2012, Texas Instruments Incorporated

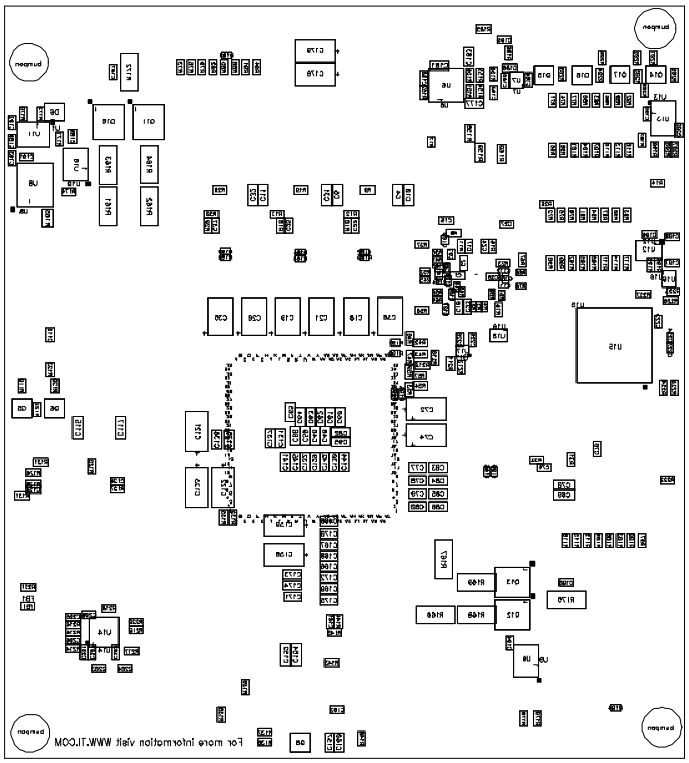


Figure 93. TPS59640EVM-751 Bottom Assembly Drawing (Bottom View)

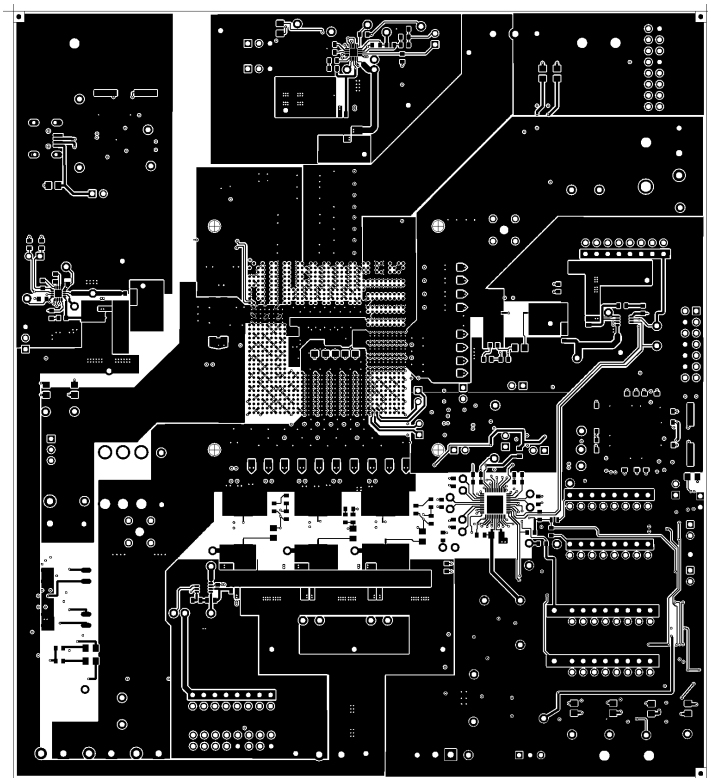


Figure 94. TPS59640EVM-751 Top Copper

Copyright © 2012, Texas Instruments Incorporated

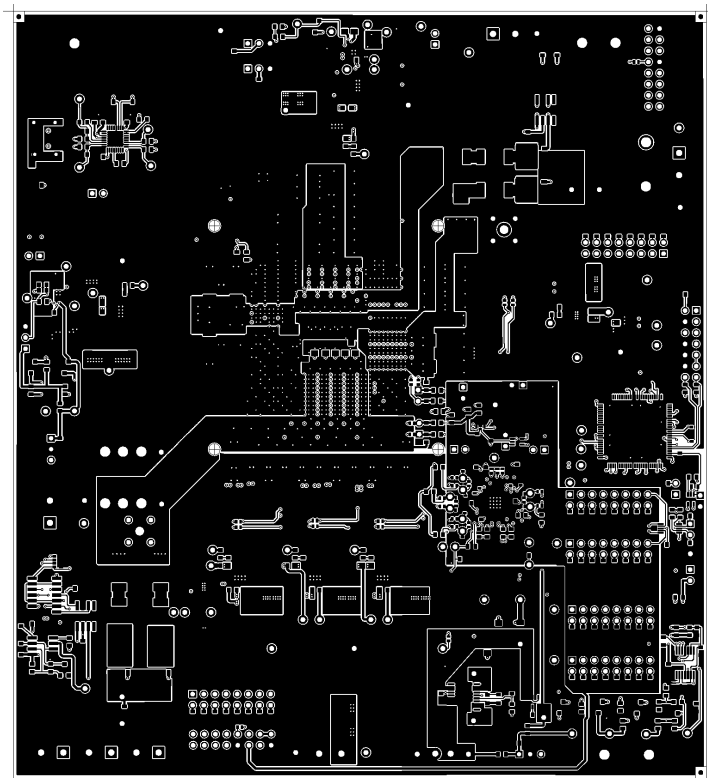


Figure 95. TPS59640EVM-751 Bottom Copper

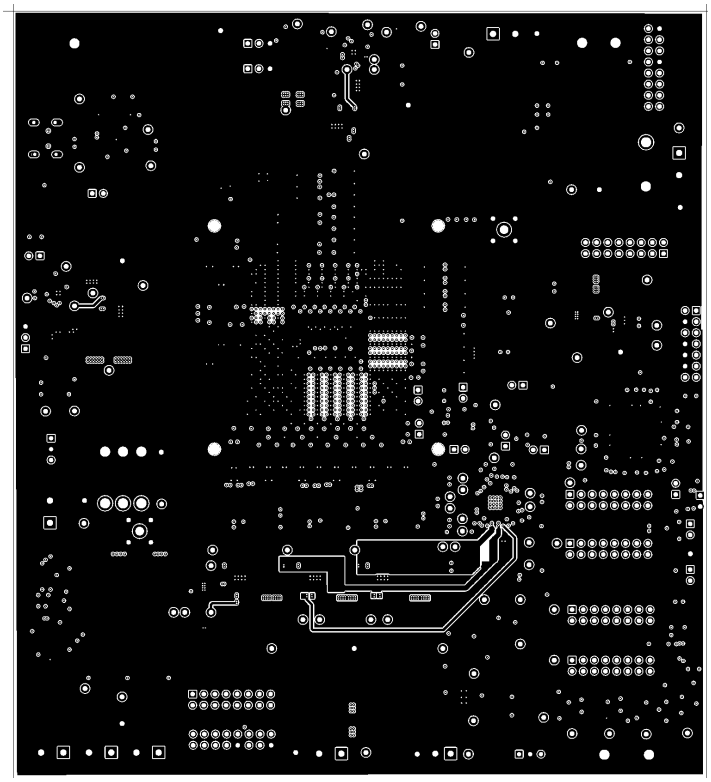


Figure 96. TPS59640EVM-751 Internal Layer 2

Copyright © 2012, Texas Instruments Incorporated

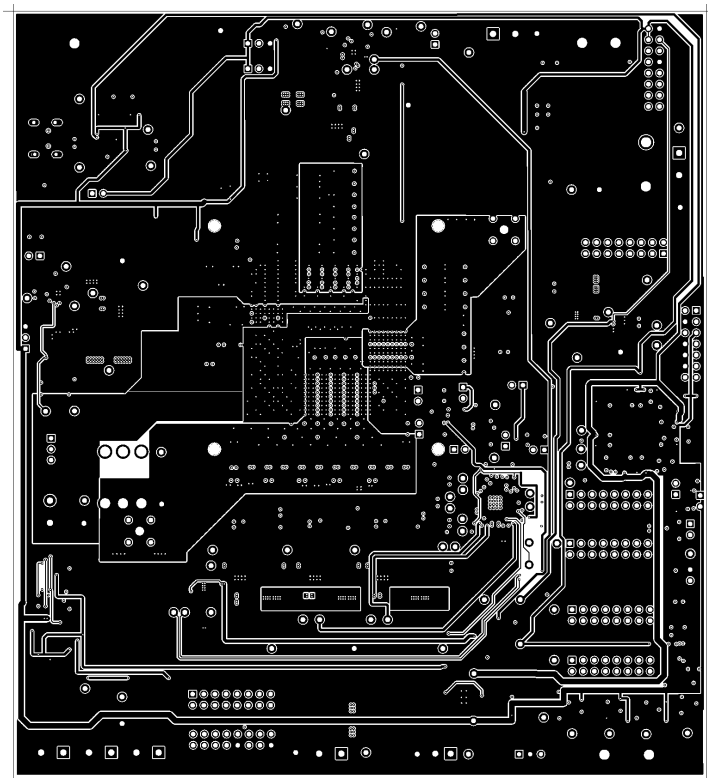


Figure 97. TPS59640EVM-751 Internal Layer 3

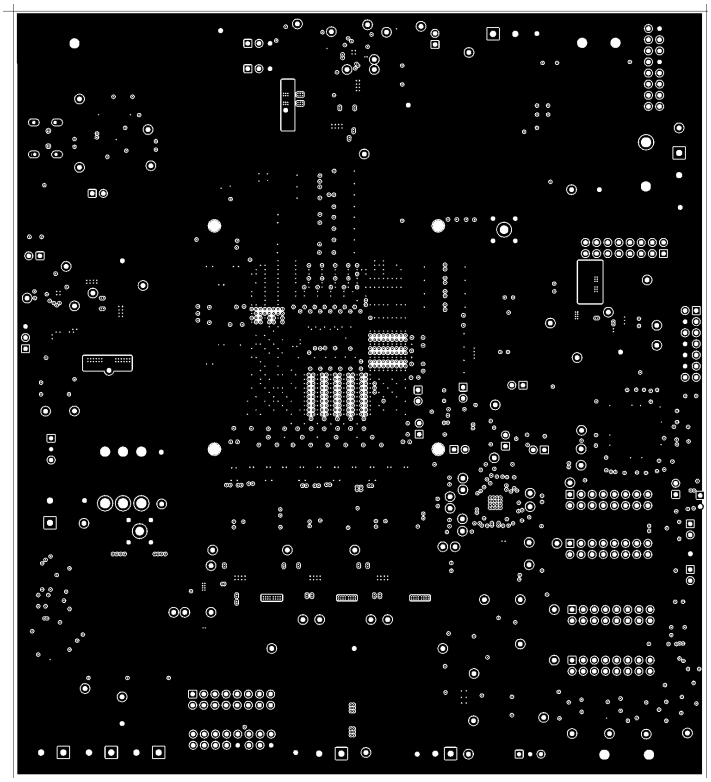


Figure 98. TPS59640EVM-751 Internal Layer 4

Copyright © 2012, Texas Instruments Incorporated

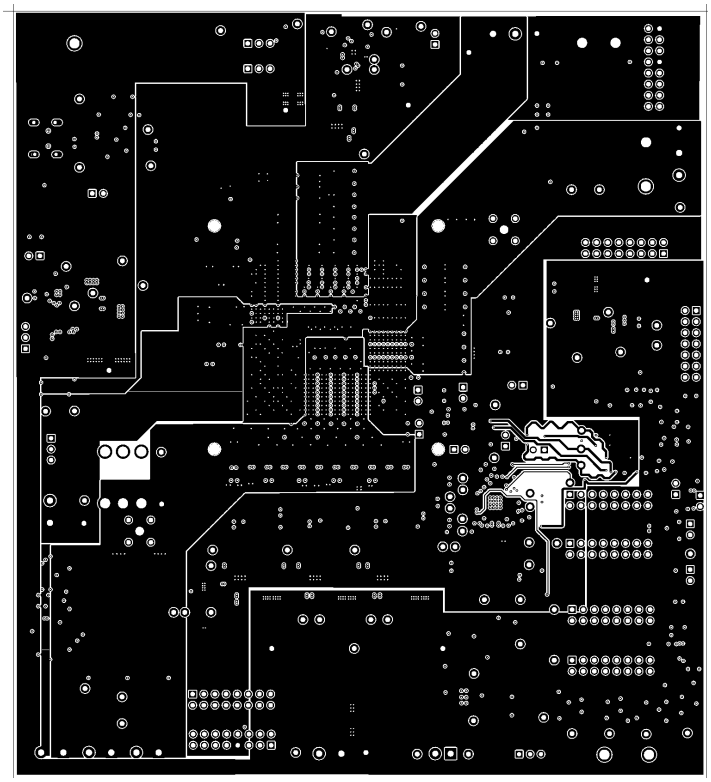


Figure 99. TPS59640EVM-751 Internal Layer 5

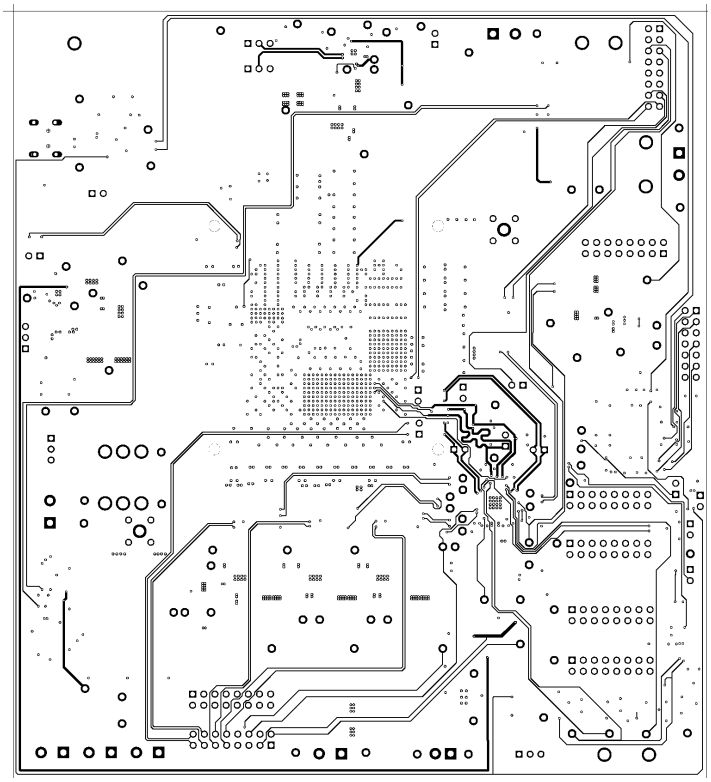


Figure 100. TPS59640EVM-751 Internal Layer 6

Copyright © 2012, Texas Instruments Incorporated

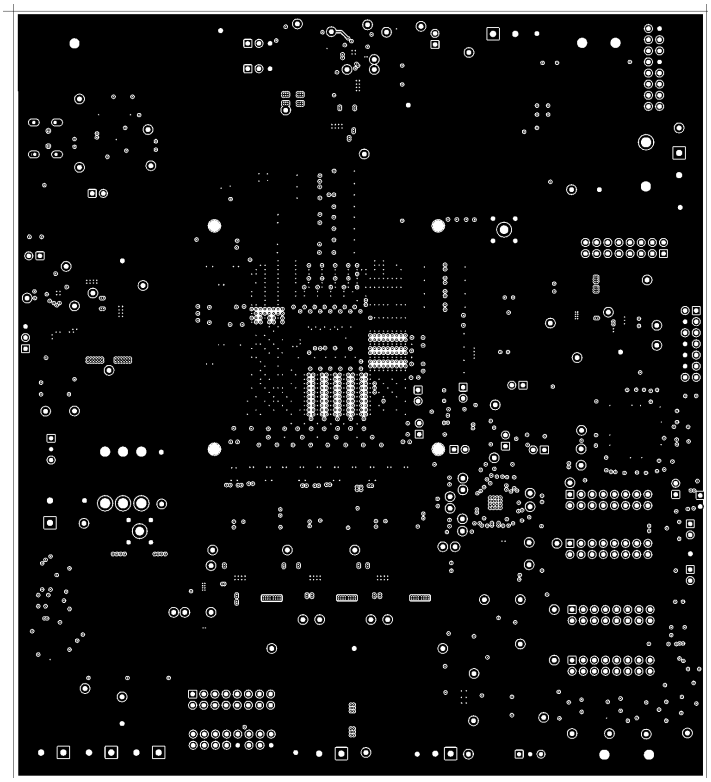


Figure 101. TPS59640EVM-751 Internal Layer 7

Copyright © 2012, Texas Instruments Incorporated

10 Bill of Materials

The EVM major components list according to the schematics shown in Figure 3 to Figure 15.

Table 13. Bill of Materials

QTY	RefDes	Description	MFR	Part Number
3	C1, C28, C163	Capacitor, Ceramic, 220nF, 25V, X7R, 10%, 0603	STD	STD
29	C119, C120, C156, C164, C180, C182, C185, C191, C192, C193, C196, C199, C201, C202, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223	Capacitor, Ceramic, 0.1uF, 25V, X7R, 10%, 0603	STD	STD
10	C12, C13, C33, C71, C113, C118, C124, C155, C176, C195	Capacitor, Ceramic, 1nF, 50V, X7R, 10%, 0603	STD	STD
2	C14, C26	Capacitor, Ceramic, 100pF, 50V, C0G, 10%, 0603	STD	STD
1	C16	Capacitor, Ceramic, 0.33uF, 25V, X7R, 10%, 0603	STD	STD
1	C160	Capacitor, Ceramic, 2.2uF, 25V, X7R, 10%, 0805	STD	STD
12	C17, C23, C24, C34, C73, C187, C188, C190, C194, C200, C225, C226	Capacitor, Ceramic, 1uF, 25V, X7R, 10%, 0603	STD	STD
4	C18, C19, C20, C21	Capacitor, Aluminum, 2.0V, 470uF, 4mohm, 20%, D2T	Sanyo	2TPLF470M4E
5	C186, C189, C207, C208, C125	Capacitor, Ceramic, 0.01uF, 25V, X7R, 10%, 0603	STD	STD
2	C197, C198	Capacitor, Ceramic, 10pF, 50V, C0G, 10%, 0603	STD	STD
6	C2, C38, C76, C127, C162, C184	Capacitor, Ceramic, 2.2uF, 25V, X7R, 10%, 0603	STD	STD
2	C205, C206	Capacitor, Ceramic, 22pF, 50V, C0G, 5%, 0603	STD	STD
1	C3	Capacitor, Ceramic, 4.7uF, 25V, X7R, 10%, 0805	STD	STD
40	C39, C40, C41, C42, C43, C44, C45, C47, C51, C52, C53, C54, C55, C56, C57, C58, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C95, C96, C128, C132, C133, C135, C137, C138, C140, C141, C142, C143, C144, C146	Capacitor, Ceramic, 22uF, 6.3V, X5R, 10%, 0805	STD	STD
24	C4, C5, C6, C7, C8, C9, C10, C11, C29, C30, C31, C32, C67, C68, C69, C70, C114, C115, C116, C117, C151, C152, C153, C154	Capacitor, Ceramic, 10uF, 25V, X7R, 20%, 1206	STD	STD
20	C46, C48, C59, C60, C61, C62, C63, C64, C65, C66, C165, C166, C167, C168, C170, C172, C157, C177, C181, C183	Capacitor, Ceramic, 10uF, 6.3V, X5R, 10%, 0805	STD	STD
5	C72, C74, C121, C122, C158	Capacitor, Aluminum, 2.0V, 330uF, 2mohm, 20%, 7343	Sanyo	2TPF330M6
4	C98, C102, C106, C110	Capacitor, Ceramic, 33nF, 25V, X7R, 10%, 0603	STD	STD
8	D1, D2, D3, D9, D10, D12, D13, D14	Diode, LED, Green Clear, 20mcd, 0.079x0.049	Lite On	LTST-C170GKT
5	D4, D5, D7, D8, D11	Diode, LED, Red Clear, 20mcd, 0.079x0.049	Lite On	LTST-C170CKT
1	D6	Diode, Schottky, 200mA, 30V, SOT-23,	Vishay-Liteon	BAT54-V-GS08
1	FB1	Bead, SMD, Ferrite, 100MHz Max, 200mA, +/-25%, 0603	WE	74279266A
4	L1, L2, L3, L4	Inductor, SMT, 0.36uH, 35A , 0.82mohm, 10x11.5mm	Toko	FCUL1040-H-R36M
2	L5, L6	Inductor, SMT, 0.56uH, 32A , 1.3mohm, 10x11.2mm	Toko	FDUE1040J-H-R56M
6	Q1, Q2, Q3, Q4, Q7, Q9	MOSFET, Synchronous Buck NexFET Power Block SON 5X6mm	TI	CSD87350Q5D
4	Q10, Q11, Q12, Q13	MOSFET, Nchan, 25V, 31A, 2.5mohm, QFN5X6mm	TI	CSD16407Q5
1	Q14	MOSFET, Pchan, -60V, -0.33A, 2ohm, SOT23	Infineon	BSS83P
6	Q5, Q6, Q8, Q15, Q16, Q17	MOSFET, Nchan, 100V, 0.17A, 6ohm, SOT23	Fairchild	BSS123
1	R1	Resistor, Chip, 71.5k, 1/10W, 1%, 0603	STD	STD
7	R119, R120, R136, R203, R204, R205, R209	Resistor, Chip, 180, 1/10W, 1%, 0603	STD	STD

Copyright © 2012, Texas Instruments Incorporated

Table 13. Bill of Materials (continued)

QTY	RefDes	Description	MFR	Part Number
19	R12, R13, R26, R30, R34, R42, R43, R54, R57, R129, R131, R133, R134, R145, R146, R148, R150, R219, R220	Resistor, Chip, 0, 1/10W, 1%, 0603	STD	STD
5	R121, R123, R140, R200, R207	Resistor, Chip, 1.00k, 1/10W, 1%, 0603	STD	STD
14	R122, R137, R138, R139, R147, R171, R174, R187, R201, R202, R206, R208, R217, R218	Resistor, Chip, 10.0k, 1/10W, 1%, 0603	STD	STD
1	R128	Resistor, Chip, 10.5k, 1/10W, 1%, 0603	STD	STD
2	R130, R141	Resistor, Chip, 37.4k, 1/10W, 1%, 0603	STD	STD
1	R14	Resistor, Chip, 169k, 1/10W, 1%, 0603	STD	STD
1	R151	Resistor, Chip, 15.0k, 1/10W, 1%, 0603	STD	STD
4	R153, R223, R224, R225	Resistor, Chip, 2.00k, 1/10W, 1%, 0603	STD	STD
1	R156	Resistor, Chip, 51.1k, 1/10W, 1%, 0603	STD	STD
1	R157	Resistor, Chip, 1, 1/10W, 1%, 0603	STD	STD
3	R158, R159, R160	Resistor, Chip, 1, 1/10W, 1%, 0805	STD	STD
7	R16, R71, R72, R73, R95, R96, R97	Resistor, Chip, 150k, 1/18W, 1%, 0603	STD	STD
3	R161, R162, R167	Resistor, Chip, 0.01, 1W, 2512	STD	STD
5	R163, R164, R166, R168, R169	Resistor, Chip, 0.05, 1W, 2512	STD	STD
1	R165	Resistor, Chip Array, 10.0k, 62.5mW, 5%, 1206	Yageo	TC164-JR-0710KL
3	R17, R181, R194	Resistor, Chip, 10.0k, 1/16W, 1%, 0402	STD	STD
1	R170	Resistor, Chip, 8.06k, 1/10W, 1%, 0603	STD	STD
2	R172, R175	Resistor, Chip, 0.005, 1W, 2512	STD	STD
5	R176, R177, R178, R179, R199	Resistor, Chip, 330, 1/10W, 1%, 0603	STD	STD
8	R180, R182, R183, R184, R188, R189, R195, R196	Resistor, Chip, 1M, 1/16W, 1%, 0402	STD	STD
1	R186	Resistor, Chip, 100, 1/10W, 1%, 0603	STD	STD
2	R192, R193	Resistor, Chip, 3.01k, 1/10W, 1%, 0603	STD	STD
7	R2, R40, R47, R53, R59, R132, R135	Resistor, Chip, 10, 1/10W, 1%, 0603	STD	STD
1	R21	Resistor, Chip, 200k, 1/10W, 1%, 0603	STD	STD
1	R211	Resistor, Chip, 75, 1/10W, 1%, 0603	STD	STD
1	R212	Resistor, Chip, 130, 1/10W, 1%, 0603	STD	STD
1	R213	Resistor, Chip, 43.2, 1/10W, 1%, 0603	STD	STD
1	R214	Resistor, Chip, 1.50k, 1/10W, 1%, 0603	STD	STD
2	R215, R216	Resistor, Chip, 33.2, 1/10W, 1%, 0603	STD	STD
1	R22	Resistor, Chip, 4.12k, 1/10W, 1%, 0603	STD	STD
2	R221, R226	Resistor, Chip, 475, 1/10W, 1%, 0603	STD	STD
1	R222	Resistor, Chip, 2.21k, 1/10W, 1%, 0603	STD	STD
1	R227	Resistor, Chip, 2.74k, 1/10W, 1%, 0603	STD	STD
1	R24	Resistor, Chip, 309k, 1/10W, 1%, 0603	STD	STD
1	R3	Resistor, Chip, 54.9, 1/16W, 1%, 0402	STD	STD
4	R35, R44, R55, R65	Resistor, Chip, 17.8k, 1/8W, 1%, 0805	STD	STD
12	R36, R41, R45, R52, R56, R64, R66, R70, R190, R191, R197, R198	Resistor, Chip, 0, 1/16W, 1%, 0402	STD	STD
4	R38, R50, R62, R68	Resistor, Chip, 162k, 1/10W, 1%, 0603	STD	STD
4	R39, R51, R63, R69	Resistor, Chip, 28.7k, 1/10W, 1%, 0603	STD	STD
1	R4	Resistor, Chip, 130, 1/16W, 1%, 0402	STD	STD
1	R6	Resistor, Chip, 8.45k, 1/10W, 1%, 0603	STD	STD
1	R7	Resistor, Chip, 42.2k, 1/10W, 1%, 0603	STD	STD
8	R74, R75, R76, R98, R99, R100, R152, R173	Resistor, Chip, 100k, 1/10W, 1%, 0603	STD	STD

Copyright © 2012, Texas Instruments Incorporated

Table 13. Bill of Materials (continued)

QTY	RefDes	Description	MFR	Part Number
6	R77, R78, R79, R101, R102, R103	Resistor, Chip, 75.0k, 1/10W, 1%, 0603	STD	STD
2	R8, R23	Resistor, Chip, 15.4k, 1/10W, 1%, 0603	STD	STD
6	R80, R81, R82, R104, R105, R106	Resistor, Chip, 56.2k, 1/10W, 1%, 0603	STD	STD
6	R83, R84, R85, R107, R108, R109	Resistor, Chip, 39.2k, 1/10W, 1%, 0603	STD	STD
8	R86, R87, R88, R110, R111, R112, R154, R155	Resistor, Chip, 30.1k, 1/10W, 1%, 0603	STD	STD
6	R89, R90, R91, R113, R114, R115	Resistor, Chip, 24.3k, 1/10W, 1%, 0603	STD	STD
12	R9, R11, R15, R19, R27, R28, R31, R33, R124, R125, R142, R143,	Resistor, Chip, 2.21, 1/10W, 1%, 0603	STD	STD
7	R92, R93, R94, R116, R117, R118, R149	Resistor, Chip, 20.0k, 1/10W, 1%, 0603	STD	STD
6	RT1, RT2, RT3, RT4, RT5, RT6	NTC Thermistor, 100k, 0603, 5%	Murata	NCP18WF104J03RB
1	U1	IC, 3+1 phase, IMVP-7 VCORE CPU and GPU Controller, QFN-48	TI	TPS59640RSL
1	U11	IC, Timer, Low-Power CMOS, SO-8	TI	TLC555CDR
1	U12	IC, Dual 10 ohm SPDT Analogy Switch, DGS_10P	TI	TS5A23157DGS
1	U13	IC, Nano Power, Open output comparators, PW14	TI	TLV3404IPW
1	U14	IC, USB to series port controller, QFN-32	TI	TUSB3410RHB
1	U15	IC, CMOS programmable controller, QFP-100	TI	TMS320F2806PZS
2	U16, U18	IC, Dual Schmitt-trigger inverter, DCK-6	TI	SN74LVC2G07DCK
1	U17	IC, Dual-bit dual-supply bus transceiver, RSW-10	TI	SN74AVC2T245RSW
2	U2, U3	IC, Dual high voltage, efficient synchronous MOSFET buck driver, QFN-8	TI	TPS51601ADRB
1	U4	IC, High performance, single synchronous step down controller, QFN-16	TI	TPS51219RTE
1	U5	IC, Complete DDR2, DDR3 and DDR3L memory power solution, QFN-20	TI	TPS51916RUK
1	U6	IC, Dual low dropout regulator, 500mA and 250mA outputs, PWP20	TI	TPS70102PWP
1	U7	IC, 150mA, low Iq, wide bandwidth, LDO, SC70	TI	TPS71712DCK
1	U8	IC, Quadruple 2-input positive –AND gates, SO-14	TI	SN74HC08D
2	U9, U10	IC, Dual 4A High speed low side power MOSFET drivers, SO-8	TI	UCC27324D
1	X1	Crystal, controlled oscillators, 0.150”x0.528”	ABRACON	ABLS-20.000MHZ-B2-T
1	Y1	Crystal, controlled oscillators, 0.150”x0.528”	ABRACON	ABLS-12.000MHZ-B2-T
0	XU1	Socket, CPU	Molex	rPGA989

Copyright © 2012, Texas Instruments Incorporated

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 20 V and the output voltage range of 0 V to 1.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 80°C. The EVM is designed to operate properly with certain components above 80°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 20 V and the output voltage range of 0 V to 1.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 80°C. The EVM is designed to operate properly with certain components above 80°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

http://www.tij.co.jp

【ご使用にあたっての注】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated